Name And Designation : VIJAYA KUMAR VADLADI ,

                              Assistant Professor.

Email ID : vijay20052009@gmail.com

Educational Details :

- M.TECH-VLSI Design (Electronics and Communication Engineering) (JNTUH-2014).
- B.Tech (Electronics and Communication Engineering) (JNTUK- 2009).
- INTERMEDIATE(MPC-2005)
- SSC(SSC-2003)

Professional Background:

- Assistant Professor, Electronics and Communication Engineering, GRIET-HYDERABAD,2013-2020(Present).

Committee Work:

NBA,JNTU INSPECTION WORK,NAAC,DISCIPLINE COMMITTEE.

Courses Taught:

- COMPUTER PROGRAMMING AND DATA STRUCTURES
- COMPUTER PROGRAMMING
- DATA STRUCTURES USING C
- ANTENNAS AND WAVE PROPAGATION
- EMTL
- PROGRAMMING, DATA STRUCTURES AND ALGORITHMS USING PYTHON (NPTEL)
- INTRODUCTION TO EMBEDDED SYSTEM DESIGN(NPTEL)
- DIGITAL COMMUNICATION LAB
- COMPUTER PROGRAMMING AND DATA STRUCTURES LAB
- COMPUTER PROGRAMMING LAB
- DATA STRUCTURES USING C LAB
- SIGNALS AND SYSTEMS LAB
- OOPS THROUGH JAVA LAB

PUBLICATIONS:

1. V.Vijaya Kumar, Implementation of 32-Bit Unsigned Multiplier Using CLAA and CSLA Published at International Journal of New Trends In Electronics and Communication,(IJNTEC – ISSN 2347-7334) Volume 02,Issue 07,October 2014.

2. V.Vijaya Kumar, A High Speed Design of 32-Bit Multiplier Using Modified CSLA Published at International Journal of Emerging Trends In Electrical and Electronics,(IJETEE –ISSN 2320-9569) Volume 10,Issue 09,October 2014.

3.V.Vijaya Kumar ,Loaded Resonent Converter for DC to DC energy conversion Published at International Journal of Advanced technology in Engineering and science ,(ISSN 2348-7550),Volume 05, Issue 03, March 2017.

4. V. Vijaya Kumar, Design Performance Dual Logic Level Multiplier Published at International Journal of Advanced technology in Engineering and science ,(ISSN 2348-7550),Volume 05, Issue 03, March 2017.

PROFESSIONAL WORK:

1.Two Week ISTE Workshop on "Computer Programming" Conducted by IIT – Bombay from may   20 th ,2014 to june 21 st 2014.

2.Participated in Workshop on "Cyber Security" under the National Mission on Education through ICT from 10-20 July 2014 at GRIET,HYD

3. Faculty Development Programme on "Guide To a Passionate Teacher" from 29 june to 04 july 2015.

4. Faculty Development Programme on "Software Defined Radio" from 16 – 17 Dec 2015.

5.Participated in FDP on "Use of ICT in Education for Online and Blended Learning " under the National Mission on Education through ICT on 14,15 June & 25,26 June 2016

6. Three day National level workshop on "Advanced Big Data Analytics with Hadoop Eco SYSTEM" from 19 th to 21 st Jan 2017.

7. Faculty Development Programme on "C and Data Structures" from 21 st -25 th Aug 2017

8. Participated in FDP on "Foundation Program in ICT for Education " conducted by IIT bombay from March 8,2018 to April 12, 2018.

9. Participated in FDP on "Pedagogy for Online and Blended teaching- learning Process " conducted by IIT bombay from May 3,2018 to May 30, 2018.

10.Participated in Workshop IITBX ESIM conducted by GRIET from 20th sep to 21th sep 2019

11.Participated in Workshop Digital Learning through WEB and CLOUD APPS conducted by GRIET from 2nd Aug to 3rd Aug 2019

12.Participated in Seminar MOODLE LEARNING MANAGEMENT SYSTEM conducted by GRIET on 2nd MAY 2020.

13.Participated in workshop CYBER SECURITY conducted by GRIET on 30th JUNE 2020.

External Examiner   :

- EDC LAB -MLRIT

AWARDS AND ACHIEVEMENTS:

Certifications

1. Microsoft Certified Educator for Technology Literacy for Educators.

2. Problem solving through programming in C, NPTEL , 2018.

3. CCNA ROUTING AND SWITCHING, 2019.

4. Introduction to Python, COURSERA, 2020.

5. Image Denoising Using Auto Encoders in Keras and Python,COURSERA,2020.

6. Python for Data Science, Cognitiveclass,2020.

7. Computer programming for everyone, university of Leeds and institute of coding,2020.