ACADEMIC REGULATIONS
PROGRAM STRUCTURE
and
DETAILED SYLLABUS

Master of Technology

(Embedded Systems)

(Two Year Regular Programme)

(Applicable for Batches admitted from 2017)

GOKARAJU RANGARAJU

INSTITUTE OF ENGINEERING AND TECHNOLOGY

(Autonomous)

ACADEMIC REGULATIONS

GOKARAJU RANGARAJU
INSTITUTE OF ENGINEERING AND TECHNOLOGY

For all Postgraduate Programmes (M.Tech)
GR17 REGULATIONS

Gokaraju Rangaraju Institute of Engineering & Technology-2017 Regulations (GR 17 Regulations) are given hereunder. These regulations govern all the Post Graduate programmes offered by various departments of Engineering with effect from the students admitted to the programmes from 2017-18 academic year.

1. **Programme Offered:** The Post Graduate programme offered by the department is M.Tech, a two-year regular programme in that discipline.

2. **Medium of Instruction:** The medium of instruction (including examinations and reports) is English.

3. **Admissions:** Admission into the M.Tech Programme in any discipline shall be made subject to the eligibility and qualifications prescribed by the University from time to time. Admissions shall be made either on the basis of the merit rank obtained by the student in PGCET conducted by the APSCHE for M. Tech Programmes or on the basis of any other order of merit approved by the University, subject to reservations as prescribed by the Government from time to time.

4. **Programme Pattern:**
   a) A student is introduced to "Choice Based Credit System (CBCS)" for which he/she has to register for the courses at the beginning of each semesters as per the procedure.
   b) Each Academic year of study is divided into two semesters.
   c) Minimum number of instruction days in each semester is 90.
   d) The total credits for the Programme is 88.
   e) Grade points, based on percentage of marks awarded for each course will form the basis for calculation of SGPA (Semester Grade Point Average) and CGPA (Cumulative Grade Point Average).
   f) A student has a choice of registering for credits from the courses offered in the programme.
   g) All the registered credits will be considered for the calculation of final CGPA.

5. **Award of M.Tech Degree:** A student will be declared eligible for the award of the M. Tech Degree if he/she fulfills the following academic requirements:
   a) A student shall be declared eligible for the award of M.Tech degree, if he/she pursues the course of study and completes it successfully in not less than two academic years and not more than four academic years.

B) A Student, who fails to fulfill all the academic requirements for the award of the degree within four academic years from the date of admission, shall forfeit his/her seat in M.Tech courses.

c) The Degree of M.Tech shall be conferred by Jawaharlal Nehru Technological University Hyderabad (JNTUH), Hyderabad, on the students who are admitted to the programme and fulfill all the requirements for the award of the degree.

6. Attendance Requirements

a) A student shall be eligible to appear for the semester end examinations if he/she puts in a minimum of 75% of attendance in aggregate in all the courses concerned in the semester.

b) Condonation of shortage of attendance in aggregate up to 10% (65% and above and below 75%) in a semester may be granted. A committee headed by Dean (Academic Affairs) shall be the deciding authority for granting the condonation.

c) Students who have been granted condonation shall pay a fee as decided by the Academic Council.

d) A candidate shall get minimum required attendance at least in three theory subjects in the semester to get promoted to the next semester. In order to qualify for the award of M.Tech. Degree, the candidate shall complete all the academic requirements of the subjects, as per the course structure.

E) Students whose shortage of attendance is not condoned in any semester are detained and are not eligible to take their end examinations of that semester. They may seek re-registration for that semester when offered next with the academic regulations of the batch into which he/she gets re-registered.

7. Paper Setting, Evaluation of Answer Scripts, Marks and Assessment

a) Paper setting and Evaluation of the Answer Scripts shall be done as per the procedures laid down by the Academic Council of the College from time to time.

b) The following is the division of marks between internal and external evaluations.

S.no	Particulars	Internal	External	Total
1	Theory	30	70	100
2	Practical	30	70	100
3	Comprehensive Viva	-	100	100
4	Seminar	30	70	100
5	Project work	30	70	100

c) The marks for internal evaluation per semester per theory course are divided as follows:

i. **For Mid written examinations: 20 Marks**
ii. **For Assignment: 5 Marks**
iii. **For Attendance: 5 Marks**
iv. **Total: 30Marks**

d) Mid-Term Written Examination: There shall be two mid-term written examinations during a semester. The first mid-term written examination shall be conducted from the first

50 per cent of the syllabus and the second mid-term written examination shall be conducted from the remaining 50 per cent of the syllabus. The mid-term written examinations shall be evaluated for **20 marks** and average of the marks scored in the two mid-term written examinations shall be taken as the marks scored by each student in the mid-term written examination for that semester.

e) **Assignment:** Assignments are to be given to the students and marks not exceeding 5 (5%) per semester per paper are to be awarded by the teacher concerned.

f) **Attendance:** A maximum of 5 marks (5%) per semester per course are to be awarded on the basis of attendance one puts in. Course-wise attendance is taken for this purpose.

g) **For Internal Evaluation in Practical/Lab Subjects:** The marks for internal evaluation are 30. Internal Evaluation is done by the teacher concerned with the help of the other staff member nominated by Head of the Department. Marks Distribution is as follows:

i.	**Writing the program/Procedure:**	**10 Marks**
ii.	**Executing the program/Procedure:**	**10 Marks**
iii.	**Viva:**	**05 Marks**
iv.	**Attendance:**	**05 Marks**
v.	**Total:**	**30Marks**

h) **For External Evaluation in Practical/Lab Subjects:** The Semester end examination shall be conducted by an external examiner and a staff member of the Department nominated by Head of the Department. Marks distribution is as follows:

i.	**Writing the program/Procedure:**	**20 Marks**
ii.	**Executing the program/Procedure:**	**20 Marks**
iii.	**Viva:**	**15 Marks**
iv.	**Lab Record:**	**15 Marks**
v.	**Total:**	**70 Marks**

i) **Evaluation of Main Project Work:** A Project Review Committee (PRC) is to be constituted by the Principal/Director with Head of the Department as the Chairman and two other senior faculty members of the department.

i. **Registration for Project work:** A candidate is permitted to register for the project work after satisfying the attendance requirements of all the courses (theory and practical courses) up to III Semester.

ii. After satisfying the registration requirements, a candidate is permitted to register for the project work after satisfying, the title, objectives and plan of action of his project work to the Project Review Committee for its approval. Only after obtaining the approval of Project Review Committee of the Department, the student can initiate the project work. Any changes thereafter in the project are to be approved by PRC. The student has to work under the guidance of both internal guide (one faculty member of the department) and external guide (from Industry not below the rank of an officer). Internal guide is allotted by the Head of the Department or Coordinator of the Project Work whereas external guide is allotted by the industrial organization in which the project is undertaken.

iii. The candidate shall submit status of the report in two stages at least with a gap of 20 days between them.

iv. The work on the project shall be initiated in the beginning of the fourth semester and the duration is one semester. A candidate is permitted to submit project report only after successful completion of theory and practical courses with the approval of PRC and not earlier than 40 days from the date of registration of the project work. For the approval of PRC the candidate shall submit the draft copy of the thesis to the Head/Coordinator (through internal research guide) and shall make an oral presentation before the PRC.

v. Two hardcopies and one soft copy of the project work (dissertation) certified by the research supervisors shall be submitted to the College/Institute.

vi. The thesis shall be adjudicated by one external examiner selected by the Institute out of 5-member panel, submitted by the department.

vii. The marks allotted for project work review are 100, out of which30 are for internal and 70 for external. Internal evaluation marks are awarded by the PRC on the basis of the student's performance in the three pre-submission reviews and the external evaluation is done by the external examiner.

viii. The marks allotted for project work and dissertation are 100, out of which 30 are for internal and 70 for external. Internal evaluation marks are awarded by the PRC on the basis of the student's performance in the three pre-submission reviews and the external evaluation is done by the external examiner. In both internal and external evaluations the student shall score at least 40% marks and an aggregate of 50% marks to pass in the project work. If the report of the examiner is favorable, Viva-voce examination shall be conducted by a Board consisting of the Supervisor, Head and the External Examiner who adjudicated the project work. The Board shall jointly evaluate the student's performance in the project work.

ix. In case the student doesn't pass through the project work, he has to reappear for the viva-voce examination, as per the recommendations of the Board. If he fails succeed at the second Viva-voce examination also, he will not be eligible for the award of the degree, unless he is asked to revise and resubmit the Project by the Board. Head of the Department and Project coordinator shall coordinate and make arrangements for the conduct of viva-¬voce examination. When one does get the required minimum marks both in internal and external evaluations the candidate has to revise and resubmit the dissertation in the time frame prescribed by the PRC. If the report of the examiner is unfavorable again, the project shall be summarily rejected.

x. If the report of the viva-voce is not satisfactory, the candidate will retake the viva-voce examination after three months. If he fails to get a satisfactory report at the second viva-voce examination, he will not be eligible for the award of the degree, unless the candidate is asked to revise and resubmit.

8. **Recounting of Marks in the End Examination Answer Books:** A student can request for re-counting of his/her answer book on payment of a prescribed fee.
9. **Re-evaluation of the End Examination Answer Books:** A student can request for re-evaluation of his/her answer book on payment of a prescribed fee.
10. **Supplementary Examinations:** A student who has failed in an end semester examination can appear for a supplementary examination, as per the schedule announced by the College/Institute.

11. Malpractices in Examinations: Disciplinary action shall be taken in case of malpractices during Mid/ End-examinations as per the rules framed by the Academic Council.

12. Academic Requirements

a) A student shall be deemed to have secured the minimum academic requirement in a subject if he / she secures a minimum of 40% of marks in the Semester-end Examination and a minimum aggregate of 50% of the total marks in the Semester-end examination and Internal Evaluation taken together.

b) A student shall be promoted to the next semester only when he/she satisfies the requirements of all the previous semesters.

c) In order to qualify for the award of M.Tech Degree, the student shall complete the academic requirements of passing in all the Courses as per the course structure including Seminars and Project if any.

d) In case a Student does not secure the minimum academic requirement in any course, he/she has to reappear for the Semester-end Examination in the course, or re-register for the same course when next offered or re-register for any other specified course, as may be required. However, one more additional chance may be provided for each student, for improving the internal marks provided the internal marks secured by a student are less than 50% and he/she failed finally in the course concerned. In the event of taking another chance for re-registration, the internal marks obtained in the previous attempt are nullified. In case of re-registration, the student has to pay the re-registration fee for each course, as specified by the College.

E) Grade Points: A 10- point grading system with corresponding letter grades and percentage of marks, as given below, is followed

Letter Grade	Grade Point	Percentage of Marks
O (Outstanding)	10	Marks>=80 and Marks <= 100
A+ (Excellent)	9	Marks>=70 and Marks < 80
A (Very Good)	8	Marks>=60 and Marks < 70
B+ (Good)	7	Marks>=55 and Marks < 60
B (Above Average)	6	Marks>=50 and Marks < 55
F (Fail)	0	Marks < 50
Ab (Absent)	0	

Earning of Credit:

A student shall be considered to have completed a course successfully and earned the credits if he/she secures an acceptable letter grade in the range O-P. Letter grade 'F' in any Course implies failure of the student in that course and no credits earned.

Computation of SGPA and CGPA:

The UGC recommends the following procedure to compute the Semester Grade Point

Average (SGPA) and Cumulative Grade Point Average (CGPA):

i) Skthe SGPA of kth semester(1 to 4) is the ratio of sum of the product of the number of credits and grade points to the total creditsof all courses registered by a student,

$$\text{SGPA } (S_k) = \sum_{i=1}^{n} (Ci * Gi) / \sum_{i=1}^{n} Ci$$

Where Ci is the number of credits of the ith course and Gi is the grade point scored by the student in the ith course and n is the number of courses registered in that semester.

ii) The CGPA is calculated in the same manner taking into account all the courses m, registered by a student over all the semesters of a programme, i.e., upto and inclusive of Sk, where k ≥ 2.

$$\text{CGPA} = \sum_{i=1}^{m} (Ci * Gi) / \sum_{i=1}^{m} Ci$$

iii) The SGPA and CGPA shall be rounded off to 2 decimal points.

13. **Award of Class:** After a student satisfies all the requirements prescribed for the completion of the Degree and becomes eligible for the award of M. Tech Degree by JNTUH, he/she shall be placed in one of the following four classes:

	Class Awarded	CGPA Secured
3.1	First class with distinction	CGPA ≥ 7.75
3.2	First Class	CGPA ≥ 6.75 and CGPA < 7.75
3.3	Second Class	CGPA ≥ 6.00 and CGPA < 6.75

14. **Withholding of Results:** If the student has not paid dues to the Institute/ University, or if any case of indiscipline is pending against him, the result of the student (for that Semester) may be withheld and he will not be allowed to go into the next Semester. The award or issue of the Degree may also be withheld in such cases.

15. **Transfer of students from the Constituent Colleges of JNTUH or from other Colleges/ Universities:** Transfer of students from the Constituent Colleges of JNTUH or from other Colleges/ Universities shall be considered only on case-to-case basis by the Academic Council of the Institute.

16. **Transitory Regulations:** Students who have discontinued or have been detained for want of attendance, or who have failed after having undergone the Degree Programme, may be considered eligible for readmission to the same or equivalent subjects as and when they are offered.

17. **General Rules**

a) The academic regulations should be read as a whole for the purpose of any interpretation.
b) In the case of any doubt or ambiguity in the interpretation of the above rules, the decision of the Academic Council is final.
c) In case of any error in the above rules and regulations, the decision of the Academic Council is final.
d) The college may change or amend the academic regulations or syllabi at any time and the

changes or amendments made shall be applicable to all the students with effect from the dates notified by the college.

GOKARAJU RANGARAJU

INSTITUTE OF ENGINEERING AND TECHNOLOGY

M.Tech (ES) PROGRAMME STRUCTURE

M.Tech (ES) **I Year-I Semester**

Sub-Code	Group	Subject	L	P	C	Int.	Ext.	Total
GR15D5072	PC	Embedded System Design	4	0	4	30	70	100
GR15D5073	PC	Microcontrollers for Embedded system Design	4	0	4	30	70	100
GR15D5074	PC	Embedded Real Time Operating Systems	4	0	4	30	70	100
	OE-I	**Open Elective – I**	**4**	**0**	**4**	**30**	**70**	**100**
	Elective I							
GR15D5075	PE	Software Defined Radio	4	0	4	30	70	100
GR15D5077	PE	VLSI Technology and Design						
GR15D5078	PE	Embedded Computing						
	Elective II							
GR15D5079	PE	Digital System Design	4	0	4	30	70	100
GR15D5080	PE	Soft Computing Techniques						
GR15D5081	PE	Advanced Operating Systems						
GR15D5082	Lab	Embedded C Lab	0	4	2	30	70	100
GR15D5173	SPW	Seminar – I	-	4	2	30	70	100
		Total Credits	**28**	**8**	**28**	**240**	**560**	**800**

M.Tech (ES) **I Year-II Semester**

Sub-Code	Group	Subject	L	P	C	Int.	Ext.	Total
GR15D5084	PC	Digital Signal Processors & Architectures	4	0	4	30	70	100
GR15D5085	PC	Embedded Networking	4	0	4	30	70	100
GR15D5086	PC	CPLD & FPGA Architectures and Applications	4	0	4	30	70	100
	OE – II	**Open Elective – II**	**4**	**0**	**4**	**30**	**70**	**100**
	Elective III							
GR15D5087	PE	Sensor and Actuators	4	0	4	30	70	100
GR15D5088	PE	Wireless Communications and Networks						
GR15D5089	PE	Network Security & Cryptography						
	Elective IV							
GR15D5090	PE	Multimedia Signal Coding	4	0	4	30	70	100
GR15D5091	PE	System on Chip Architecture						
GR15D5092	PE	Wireless LANs and PANs						
GR15D5093	Lab	Embedded System Lab	0	4	2	30	70	100
GR15D5174	SPW	Seminar – II	-	4	2	30	70	100
		Total	**24**	**8**	**28**	**240**	**560**	**800**

II Year-I Semester

Sub-Code	Group	Subject	L	P	C	Int.	Ext.	Total
GR15D5175	SPW	Comprehensive Viva-voce	-	-	4	0	100	100
GR15D5176	SPW	Project work Review	-	-	12	30	70	100
		Total	**-**	**-**	**16**	**30**	**170**	**200**

II Year-II Semester

Sub-Code	Group	Subject	L	P	C	Int.	Ext.	Total
GR15D5177	SPW	Project work and Dissertation	-	-	16	30	70	100
		Total			**16**	**30**	**70**	**100**

A student has a choice to select one Open Elective Pool I in I Semester and one Open Elective Pool II in II Semester.

Open Elective Pool-I

Sub-Code	Group	Subject	L	P	C	Int.	Ext.	Total
GR15D5178	OE-I	E- Commerce and Applications (CSE)	4	0	4	30	70	100
GR15D5179		Enterprise Resource Planning (IT)	4	0	4	30	70	100
GR15D5180		Modern Control Theory (EEE)	4	0	4	30	70	100
GR15D5181		Computer - Oriented Numerical Methods in Engineering (CE)	4	0	4	30	70	100
GR15D5182		Advanced Computer Architecture (ECE)	4	0	4	30	70	100
GR15D5183		Operations Research (ME)	4	0	4	30	70	100

Open Elective Pool-II

Sub-Code	Group	Subject	L	P	C	Int.	Ext.	Total
GR15D5184	OE-II	Human Computer Interaction (CSE)	4	0	4	30	70	100
GR15D5185		Big Data and Analytics (IT)	4	0	4	30	70	100
GR15D5186		Neural and Fuzzy Systems (EEE)	4	0	4	30	70	100
GR15D5187		Project Management (CE)	4	0	4	30	70	100
GR15D5188		Hardware Software Co-Design(ECE)	4	0	4	30	70	100
GR15D5189		Non-Conventional Energy Resources(ME)	4	0	4	30	70	100

I- SEMESTER

GOKARAJU RANGARAJU

INSTITUTE OF ENGINEERING AND TECHNOLOGY

EMBEDDED SYSTEMS DESIGN

M.Tech (ES) | I Year - I Semester

Course Code: GR17D5072 | L/T/P/C :3/1/0/4

COURSE OBJECTIVES

- To introduce the difference between embedded systems and general purpose systems
- To optimize hardware designs of custom single-purpose processors.
- To compare different approaches in optimizing general-purpose processors.
- To introduce different peripheral interfaces to embedded systems. .
- To apply knowledge gained in software-hardware integration in team-based projects.

COURSE OUTCOMES: After going through this course the student will be able to

- Compare Embedded system design models using different processor technologies (single-purpose, general-purpose, application specific processors).
- Describe and compare the various types of peripherals used in embedded systems
- Analyze a given embedded system design and identify its performance critical points
- Use modern engineering tools necessary for integrating software and hardware components in embedded system designs.
- Familiarize Embedded Firmware Design Approaches and Development Languages
- Utilize a top-down modular design process to complete a medium complexity embedded
- system design project under instructor specified design constraints.
- Decide which operating system/real time operating system is best suitable for the decided embedded application.

UNIT-I

Introduction to Embedded Systems: Definition of Embedded System, Embedded Systems Vs General Computing Systems, History of Embedded Systems, Classification, Major Application Areas, Purpose of Embedded Systems, Characteristics and Quality Attributes of Embedded Systems.

UNIT-II

Typical Embedded System: Core of the Embedded System: General Purpose and Domain Specific Processors, ASICs, PLDs, Commercial Off-The-Shelf Components (COTS), Memory: ROM, RAM, Memory according to the type of Interface, Memory Shadowing, Memory selection for Embedded Systems, Sensors and Actuators, Communication Interface: Onboard and External Communication Interfaces.

UNIT-III

Embedded Firmware: Reset Circuit, Brown-out Protection Circuit, Oscillator Unit, Real Time Clock, Watchdog Timer, Embedded Firmware Design Approaches and Development Languages.

UNIT-IV

RTOS Based Embedded System Design: Operating System Basics, Types of Operating Systems, Tasks, Process and Threads, Multiprocessing and Multitasking, Task Scheduling.

UNIT-V

Task Communication: Shared Memory, Message Passing, Remote Procedure Call and Sockets, Task Synchronization: Task Communication/Synchronization Issues, Task Synchronization Techniques, Device Drivers, How to Choose an RTOS.

TEXT BOOKS

1. Introduction to Embedded Systems - Shibu K.V, Mc Graw Hill.

REFERENCE BOOKS

1. Embedded Systems - Raj Kamal, TMH.
2. Embedded System Design - Frank Vahid, Tony Givargis, John Wiley.
3. Embedded Systems – Lyla, Pearson, 2013
4. An Embedded Software Primer - David E. Simon, Pearson Education.

GOKARAJU RANGARAJU

INSTITUTE OF ENGINEERING AND TECHNOLOGY

MICROCONTROLLERS FOR EMBEDDED SYSTEM DESIGN

M.Tech (ES) I Year - I Semester

Course Code: GR17D5073 L/T/P/C :3/1/0/4

COURSE OBJECTIVES

- To introduce the outline architecture of ARM7 microcontroller including basics of pipelines, registers, exception modes.
- To set up and customize a microcontroller development environment.
- To give an overview of system peripherals which cover bus structure, memory map, register programming and much more.
- To write programs that interact with other devices.
- To learn the Memory Management of RISC Microcontrollers.

COURSE OUTCOMES: After going through this course the student will be able to

- An ability to understand the hardware implementation of the ARM7 microcontrollers.
- An ability to Integrate peripherals based on I/O functions.
- An ability to learn the concept of pipelines, registers and exception modes
- An ability to program in ARM and THUMB modes.
- An ability to interpret the functions of Memory Management Unit (MMU).
- An ability to compare the performance of various ARM families of Microcontrollers.
- An ability to know the software development flow and working with projects.

UNIT-I

ARM Architecture: ARM Design Philosophy, Registers, Program Status Register, Instruction Pipeline, Interrupts and Vector Table, Architecture Revision, ARM Processor Families.

UNIT -II

ARM Programming Model – I: Instruction Set: Data Processing Instructions, Addressing Modes, Branch, Load, Store Instructions, PSR Instructions, Conditional Instructions.

UNIT –III:

ARM Programming Model – II: Thumb Instruction Set: Register Usage, Other Branch Instructions, Data Processing Instructions, Single-Register and Multi Register Load-Store Instructions, Stack, Software Interrupt Instructions

UNIT –IV:

ARM Programming: Simple C Programs using Function Calls, Pointers, Structures, Integer and Floating Point Arithmetic, Assembly Code using Instruction Scheduling, Register Allocation, Conditional Execution and Loops.

UNIT –V

Memory Management: Cache Architecture, Polices, Flushing and Caches, MMU, Page Tables, Translation, Access Permissions, Context Switch.

TEXT BOOKS

1. ARM Systems Developer's Guides- Designing & Optimizing System Software – Andrew N. Sloss, Dominic Symes, Chris Wright, 2008, Elsevier.

REFERENCE BOOKS

1. Embedded Microcomputer Systems, Real Time Interfacing – Jonathan W. Valvano – Brookes / Cole, 1999, Thomas Learning.

GOKARAJU RANGARAJU

INSTITUTE OF ENGINEERING AND TECHNOLOGY

EMBEDDED REAL TIME OPERATING SYSTEMS

M.Tech (ES) I Year - I Semester

Course Code: GR17D5074 L/T/P/C :3/1/0/4

COURSE OBJECTIVES

- To use Unix/Linux operating system as the working platform for embedded system development.
- To demonstrate system programming for input output file operations and process control operations.
- To demonstrate coding techniques involving multiprocessing.
- To apply the techniques of establishing synchronization among different tasks.
- To apply the coding techniques for the embedded applications involving interrupts and real time responses.
- To judge about which particular real time operating system is best suitable for the underlined application.
- To outline the features of different existing Real Time Operating Systems.

COURSE OUTCOMES: After going through this course the student will be able to

- Students will be able to operate on a Unix/Linux operating system for embedded system application code development.
- Students will be skilful to perform some basic level system programming.
- Students will acquire the techniques for coding applications involving multiprocessing using the real time operating system provided functions.
- Students will be equipped with the coding techniques to establish synchronization in embedded systems involving multiprocessing.
- Students will acquire the skills to design and deal with the real time embedded applications with/without interrupts.
- Students will be in a position to recommend about an operating system/real time operating system for the decided embedded application.
- Students will be able to compare the different Real Time Operating Systems and can choose the best one for the underlined embedded application.

UNIT – I

Introduction: Introduction to UNIX/LINUX, Overview of Commands, File I/O (open, create, close, lseek, read, write), Process Control (fork, vfork, exit, wait, waitpid, exec).

UNIT - II

Real Time Operating Systems: Brief History of OS, Defining RTOS, The Scheduler, Objects, Services, Characteristics of RTOS, Defining a Task, Task States and Scheduling, Task Operations,

Structure, Synchronization, Communication and Concurrency. Defining Semaphores, Operations and Use, Defining Message Queue, States, Content, Storage, Operations and Use

UNIT - III

Objects, Services and I/O: Pipes, Event Registers, Signals, Other Building Blocks, Component Configuration, Basic I/O
Concepts, I/O Subsystem

UNIT - IV

Exceptions, Interrupts and Timers: Exceptions, Interrupts, Applications, Processing of Exceptions and Spurious Interrupts, Real Time Clocks, Programmable Timers, Timer Interrupt Service Routines (ISR), Soft Timers, Operations.

UNIT - V

Case Studies of RTOS: RT Linux, MicroC/OS-II, Vx Works, Embedded Linux, Tiny OS, and Basic Concepts of Android OS.

TEXT BOOKS

1. Real Time Concepts for Embedded Systems – Qing Li, Elsevier, 2011

REFERENCE BOOKS

1. Embedded Systems- Architecture, Programming and Design by Rajkamal, 2007, TMH.
2. Advanced UNIX Programming, Richard Stevens
3. Embedded Linux: Hardware, Software and Interfacing – Dr. Craig Hollabaugh

GOKARAJU RANGARAJU

INSTITUTE OF ENGINEERING AND TECHNOLOGY

SOFTWARE DEFINED RADIO
(Elective -I)

M.Tech (ES) I Year - I Semester

Course Code: GR17D5075 L/T/P/C :3/1/0/4

COURSE OBJECTIVES

- To study and possess the knowledge on radio-frequency implementation Issues
- To study and possess the knowledge on multi-rate signal processing and digital generation of signals vital to software defined radio
- To study and possess the knowledge on ideal and practical A-to-D and D-to-A converters and To study and possess the knowledge on smart antennas.
- To have a discussion on digital hardware issues.
- To carry out case studies of SDRs.

COURSE OUTCOMES: After going through this course the student will be able to

- To apply the digital domain for the design of RF amplifiers.
- To channelize the operating band into various communication channels.
- To create arbitrary modulations directly within the digital domain.
- To incorporate sophisticated algorithms such as smart antennas into the radio to enhance performance.
- To design direct digital synthesizer.
- To design up converters and down converters
- To design a software-defined radio.

UNIT-I

Introduction to Software-Defined Radio (SDR) and Radio-Frequency Implementation Issues: A traditional radio architecture, What Is a Software Radio?, The Need for Software Radios, Characteristics and Benefits of a Software Radio. , basic SDR block diagram, Design Principles of a Software Radio, 2G architecture, hybrid radio architecture, The Purpose of the RF Front-End. Dynamic Range: The Principal Challenge of Receiver Design. RF Receiver Front-End Topologies. Enhanced Flexibility of the RF Chain with Software Radios. Importance of the Components to Overall Performance. Transmitter Architectures and Their Issues. Noise and Distortion in the RF Chain. ADC and DAC Distortion, 3G RF performance requirements..

UNIT-II

Multirate Signal Processing and Digital Generation of Signals: Introduction to Multi-rate Signal Processing, Sample Rate Conversion Principles. Polyphase Filters. Digital Filter Banks. Timing Recovery in Digital Receivers Using Multirate Digital Filters. Introduction to Digital Generation of Signals. Comparison of Direct Digital Synthesis with Analog Signal Synthesis. Approaches to

Direct Digital Synthesis. Analysis of Spurious Signals. Spurious Components due to Periodic Jitter. Bandpass Signal Generation. Performance of Direct Digital Synthesis Systems. Hybrid DDS-PLL Systems. Applications of direct Digital Synthesis. Generation of Random Sequences.

UNIT-III

Analog to Digital (A-to-D)I and Digital to Analog Conversions and Smart antennas:
Introduction to A-to-D conversion, parameters of ideal data converters, parameters of practical data converters, techniques to improve data converter performance. Introduction to Smart antennas, Vector channel modeling, benefits of smart antennas, Structures for beamforming systems, smart antenna algorithms, diversity and space-time adaptive signal processing 3G smart antenna requirements and smart antenna architectures.

UNIT-IV

Digital hardware components and Digital hardware choice:
Digital frequency up-and down- converters, digital NCO, digital mixers, cascading of digital converters and digital frequency converters, 3G transmitter requirements. Introduction to digital hardware choice, DSP processors, Field programmable arrays, Trade-offs in using DSPs, FPGAs and ASICs, power management issues, using combination of DSPs FPGAs and ASICs.

UNIT-V

Software Architecture and SDR Case Studies: Major software architecture choices, hardware-specific software architecture, software standards for SDR, Software design
patterns. Introduction and a historical perspective of SDR, SPEAKeasy I, SPEAKeasy II, SPEAKeasy III, JTRS, Wireless information Transfer system, SDR -3000 digital transceiver system, 3G SDR testbeds and 3G networks.

TEXT BOOKS

1. Jeffrey H. Reed, “Software Radio: A Modern Approach to Radio Engineering” Pearson Education Asia, 2002 (I-V).
2. Paul Burns, Software-defind radio for 3G. Artech House 2002.(I-III and V)

REFERENCE BOOKS

1. Abrie, Pieter L D Design of RF and Microwave Amplifiers and oscillators, Artech House. 1999
2. Dixon, Robert, Radio Receiver Design, Marcel Dekker, 1998.
3. JohnG Proiakis, Dimiritis G Manolakis Digital Signal Processing: Principles, Algorithms, Applications Prentice Hall, 4th edition
4. Frank B Gross, Smart antennas with Matlab
5. Richard Johnson Jr, Willaim A Sethares, Andrew G Klein, Software Receiver Design, Cambridge University Press, 2011
6. RF and DSP for SDR, Elsevier newness Press, 2008
7. P kenington, RF and baseband techniques for software defined radio, Artech House 2005.

GOKARAJU RANGARAJU

INSTITUTE OF ENGINEERING AND TECHNOLOGY

VLSI TECHNOLOGY AND DESIGN

(ELECTIVE -I)

M.Tech (ES) I Year - I Semester

Course Code: GR17D5077 L/T/P/C :3/1/0/4

COURSE OBJECTIVES

- To enable the student to visualize MOS fabrication technologies and to understand electrical properties of MOS, CMOS and Bi CMOS circuits.
- To train the student to draw integrated circuit layouts following design rules.
- To enable the student designcombinational circuit, do verification,power optimization and network testing.
- To enable the student to use power optimization techniques, design validation procedures and testing of sequential circuits.
- To train the student to use different floor planning methods and different low power architectures.

COURSE OUTCOMES: After going through this course the graduate student will be able to

- Visualize the steps taken for MOS fabrication technologies.
- Analyze electrical behaviorof MOS, CMOS and Bi CMOS circuits.
- Draw the layout of integrated circuits following design rules.
- Able to design combinational circuit.
- Design sequential circuits using different clocking disciplines.
- Carry out power optimization techniques, design validation procedure and testing of circuits.
- Carry out floor planning for different low power architectures.

UNIT-I

Review of Microelectronics and Introduction to MOS Technologies: MOS, CMOS, BiCMOS Technology, Basic Electrical Properties of MOS, CMOS & BiCMOS Circuits: Ids – Vds relationships, Threshold Voltage Vt, gm, gds and ωo, Pass Transistor, MOS, CMOS & Bi CMOS Inverters, Zp.u/Zp.d, MOS Transistor circuit model, Latch-up in CMOS circuits.

UNIT-II

Layout Design and Tools: Transistor structures, Wires and Vias, Scalable Design rules, Layout Design tools.

Logic Gates & Layouts: Static Complementary Gates, Switch Logic, Alternative Gate circuits, Low power gates, Resistive and Inductive interconnect delays.

UNIT –III

Combinational Logic Networks: Layouts, Simulation, Network delay, Interconnect design,

Power optimization, Switch logic networks, Gate and Network testing.

UNIT –IV

Sequential Systems: Memory cells and Arrays, Clocking disciplines, Design, Power optimization, Design validation and testing.

UNIT -V

Floor Planning: Floor planning methods, Global Interconnect, Floor Plan Design, Off-chip connections.

TEXT BOOKS

1. Essentials of VLSI Circuits and Systems, K. EshraghianEshraghian. D, A. Pucknell, 2005, PHI.
2. Modern VLSI Design – Wayne Wolf, 3rd Ed., 1997, Pearson Education.

REFERENCE BOOKS

1. Introduction to VLSI Systems: A Logic, Circuit and System Perspective – Ming-BO Lin, CRC Press, 2011.
2. Principals of CMOS VLSI Design – N.H.E Weste, K. Eshraghian, 2nd Ed., Addison Wesley.

GOKARAJU RANGARAJU
INSTITUTE OF ENGINEERING AND TECHNOLOGY

EMBEDDED COMPUTING
(Elective – I)

M.Tech (ES) I Year - I Semester
Course Code: GR17D5078 L/T/P/C :3/1/0/4

COURSE OBJECTIVES

- To demonstrate the student to program on linux platform.
- To have an outline on operating systems.
- To explain the overview of software development tools.
- To illustrate different interfacing modules.
- To explain the basics of networking.
- To compare various network security techniques.
- To summarize IA32 Instruction set and explain the students to work with simulation and debugging tools.

COURSE OUTCOMES: After going through this course the student will be able to

- An ability to develop programming on linux platform.
- To analyse operating system overview.
- An ability to design using various software development tools.
- To analyse interfacing modules.
- To interpret basics of networking
- To distinguish various network security techniques.
- An ability to work with simulation and debugging tools.

UNIT-I

Programming on Linux Platform: System Calls, Scheduling, Memory Allocation, Timers, Embedded Linux, Root File System, Busy Box. Operating System Overview: Processes, Tasks, Threads, Multi-Threading, Semaphore,
Message Queue.

UNIT –II

Introduction to Software Development Tools: GNU GCC, make, gdb, static and dynamic linking, C libraries, compiler options, code optimization switches, lint, code profiling tools,.

UNIT –III:

Interfacing Modules: Sensor and actuator interface, data transfer and control, GPS, GSM module interfacing with data processing and display, OpenCV for machine vision, Audio signal processing.

UNIT-IV

Networking Basics: Sockets, ports, UDP, TCP/IP, client server model, socket programming, 802.11, Bluetooth, ZigBee, SSH, firewalls, network security.

UNIT –V

IA32 Instruction Set: application binary interface, exception and interrupt handling, interrupt latency, assemblers, assembler directives, macros, simulation and debugging tools.

TEXT BOOKS

1. Modern Embedded Computing - Peter Barry and Patrick Crowley, 1st Ed., Elsevier/Morgan Kaufmann, 2012.
2. Linux Application Development - Michael K. Johnson, Erik W. Troan, Adission Wesley, 1998.
3. Assembly Language for x86 Processors by Kip R. Irvine
4. Intel® 64 and IA-32 Architectures Software Developer Manuals

REFERENCE BOOKS

1. Operating System Concepts by Abraham Silberschatz, Peter B. Galvin and Greg Gagne.
2. The Design of the UNIX Operating System by Maurice J. Bach Prentice-Hall
3. UNIX Network Programming by W. Richard Stevens

GOKARAJU RANGARAJU

INSTITUTE OF ENGINEERING AND TECHNOLOGY

DIGITAL SYSTEM DESIGN
(ELECTIVE -II)

M.Tech (ES) I Year - I Semester

Course Code: GR17D5079 L/T/P/C :3/1/0/4

COURSE OBJECTIVES

- Learn digital design of Sequential Machines.
- Learn drawing state graphs.
- Learn realization and implementation of SM Charts.
- Learn Fault modeling and test pattern generation of Combinational circuits.
- Learn fault diagnosis in sequential circuits and understand machine design, identification of fault detection experiment.

COURSE OUTCOMES: After going through the course students will be able to

- Create understanding of the design techniques of sequential Machines.
- Create understanding of the fundamental concepts of PLD's, design of FPGA's.
- Learn implementation of SM charts in combinational and sequential circuits.
- Develop skills in modelling fault free combinational circuits.
- Develop skills in modelling Sequential circuits in terms of reliability, availability and safety.
- Develop skills in modelling fault detection experiments of sequential circuits.
- Develop skills in modelling combinational circuits in terms of reliability, availability and safety.

UNIT -I

Minimization and Transformation of Sequential Machines: The Finite State Model – Capabilities and limitations of FSM – State equivalence and machine minimization – Simplification of incompletely specified machines. Fundamental mode model – Flow table – State reduction – Minimal closed covers – Races, Cycles
and Hazards.

UNIT -II

Digital Design: Digital Design Using ROMs, PALs and PLAs, BCD Adder, 32 – bit adder, State graphs for control circuits, Scoreboard and Controller, A shift and add multiplier, Array multiplier, Keypad Scanner, Binary divider.

UNIT -III

SM Charts: State machine charts, Derivation of SM Charts, Realization of SM Chart, Implementation of Binary Multiplier, dice game controller.

UNIT -IV

Fault Modeling& Test Pattern Generation: Logic Fault model – Fault detection & Redundancy-Fault equivalence and fault location –Fault dominance – Single stuck at fault model – Multiple stuck at fault models –Bridging fault model. Fault diagnosis of combinational circuits by conventional methods – Path sensitization techniques, Boolean Difference method – Kohavi algorithm – Test algorithms – D algorithm, PODEM, Random testing, Transition count testing, Signature analysis and test bridging faults.

UNIT -V

Fault Diagnosis in Sequential Circuits: Circuit Test Approach, Transition Check Approach – State identification and fault detection
experiment, Machine identification, Design of fault detection experiment

TEXT BOOKS

1. Fundamentals of Logic Design – Charles H. Roth, 5th Ed., Cengage Learning.
2. Digital Systems Testing and Testable Design – MironAbramovici, Melvin A. Breuer and Arthur D. Friedman- John Wiley & Sons Inc.
3. Logic Design Theory – N. N. Biswas, PHI

REFERENCE BOOKS

1. Switching and Finite Automata Theory – Z. Kohavi , 2nd Ed., 2001, TMH
2. Digital Design – Morris Mano, M.D.Ciletti, 4th Edition, PHI.
3. Digital Circuits and Logic Design – Samuel C. Lee, PHI

GOKARAJU RANGARAJU

INSTITUTE OF ENGINEERING AND TECHNOLOGY

SOFT COMPUTING TECHNIQUES
(ELECTIVE-II)

M.Tech (ES) I Year - I Semester

Course Code: GR17D5080 L/T/P/C :3/1/0/4

COURSE OBJECTIVES

- Identify to soft computing concepts and techniques and foster their abilities in designing and implementing soft computing based solutions for real-world and engineering problems.
- Illustrate necessary mathematical background for understanding and implementing soft computing Techniques, such as neural networks, fuzzy systems, genetic algorithms etc.
- Relate of the neural networks with supervised and unsupervised learning networks.
- Discriminate the basic principle behind the fuzzy set theory and Comprehend neuro fuzzy modeling.
- Evolution the criteria for selecting computational techniques like Genetic/ Evolutionary algorithms, Artificial Neural Networks, Fuzzy Systems, Machine learning and probabilistic reasoning etc for a particular application.
- Interpret physical principles applied in optimization algorithms concepts and their relations.
- Define case studies where soft computing techniques can be implemented.

COURSE OUTCOMES: After going through this course the student will be able to

- Implement numerical methods in soft computing.
- Apply knowledge of computing, sciences and mathematics to solve computerengineering problems
- The modern techniques and engineering tools necessary for computer engineering practices.
- Design experiments, gather/acquire, analyze, interpret data and make decisions to understand computing requirements.
- Describe, analyze and design digital computing and representation systems.
- Relate appropriate computer engineering concepts and programming languages in solving computing problems.
- apply Genetic/ Evolutionary algorithms, Artificial Neural Networks, Fuzzy Systems, Machine learning and probabilistic reasoning etc as computational tools to solve a variety of problems in various area of interest ranging from Optimization problems to Text Analytics.

UNIT –I

Introduction: Approaches to intelligent control, Architecture for intelligent control, Symbolic reasoning system, Rule-based systems, the AI approach, Knowledge representation - Expert systems.

UNIT –II

Artificial Neural Networks: Concept of Artificial Neural Networks and its basic mathematical model, McCulloch-Pitts neuron model, simple perceptron, Adaline and Madaline, Feed-forward Multilayer Perceptron, Learning and Training the neural network, Data Processing: Scaling, Fourier transformation, principal-component analysis and wavelet transformations, Hopfield network, Self-organizing network and Recurrent network, Neural Network based controller.

UNIT –III

Fuzzy Logic System: Introduction to crisp sets and fuzzy sets, basic fuzzy set operation and approximate reasoning, Introduction to fuzzy logic modeling and control, Fuzzification, inferencing and defuzzification, Fuzzy knowledge and rule bases, Fuzzy modeling and control schemes for nonlinear systems, Selforganizing fuzzy logic control, Fuzzy logic control for nonlinear time delay system.

UNIT –IV

Genetic Algorithm: Basic concept of Genetic algorithm and detail algorithmic steps, Adjustment of free parameters, Solution of typical control problems using genetic algorithm, Concept on some other search techniques like Tabu search and Ant-colony search techniques for solving optimization problems.

UNIT –V

Applications: GA application to power system optimisation problem, Case studies: Identification and control of linear and nonlinear dynamic systems using MATLAB-Neural Network toolbox, Stability analysis of Neural-Network interconnection systems, Implementation of fuzzy logic controller using MATLAB fuzzy-logic toolbox, Stability analysis of fuzzy control systems.

TEXT BOOKS

1. Introduction to Artificial Neural Systems - Jacek.M.Zurada, Jaico Publishing House, 1999.
2. Neural Networks and Fuzzy Systems - Kosko, B., Prentice-Hall of India Pvt. Ltd., 1994.

REFERENCE BOOKS

1. Fuzzy Sets, Uncertainty and Information - Klir G.J. & Folger T.A., Prentice-Hall of India Pvt. Ltd., 1993.
2. Fuzzy Set Theory and Its Applications - Zimmerman H.J. Kluwer Academic Publishers, 1994.
3. Introduction to Fuzzy Control - Driankov, Hellendroon, Narosa Publishers.
4. Artificial Neural Networks - Dr. B. Yagananarayana, 1999, PHI, New Delhi.

GOKARAJU RANGARAJU
INSTITUTE OF ENGINEERING AND TECHNOLOGY

ADVANCED OPERATING SYSTEMS
(ELECTIVE-II)

M.Tech (ES) I Year - I Semester

Course Code: GR17D5081 L/T/P/C :3/1/0/4

COURSE OBJECTIVES

- To learn the fundamentals, purpose, structure and functions of operating systems.
- To understand how the operating system abstractions can be used in the development of application programs, or to build higher level abstractions.
- To gain insight on to the distributed resource management components viz. the algorithms for implementation of distributed shared memory and commit protocols.
- To gain knowledge on Distributed operating system concepts that includes architecture, Mutual exclusion algorithms.
- To explain how to characterize and cope with processor deadlock, including prevention, avoidance, detection, and recovery.
- To know the components and management aspects of Real time, Mobile operating systems.
- To provide experience in low-level systems programming in a realistic development environment.

COURSE OUTCOMES: After going through this course the student will be able to

- An ability to describe the basic principles used in the design of modern operating systems.
- An ability to understand the difference between different types of modern operating systems, virtual machines and their structure of implementation and applications.
- An ability to understand the difference between process & thread and use of locks, semaphores, monitors for synchronizing multiprogramming with multithreaded systems.
- An ability to distinguish between various resource management techniques for distributed systems.
- An ability to understand the concepts of deadlock in operating systems and how they can be managed / avoided and implement them in multiprogramming system.
- An ability to identify the different features of real time and mobile operating systems.
- An ability to modify existing open source kernels in terms of functionality or features used.

UNIT –I

Introduction to Operating Systems: Overview of computer system hardware, Instruction execution, I/O function, Interrupts, Memory hierarchy, I/O Communication techniques, Operating system objectives and functions, Evaluation of operating System

UNIT –II

Introduction to UNIX and LINUX: Basic commands & command arguments, Standard input, output, Input / output redirection, filters and editors, Shells and operations

UNIT –III

System Calls: System calls and related file structures, Input / Output, Process creation & termination. Inter Process Communication
Introduction, file and record locking, Client – Server example, pipes, FIFOs, Streams & Messages, Name Spaces, Systems V IPC, Message queues, Semaphores, Shared Memory, Sockets & TLI.

UNIT –IV

Introduction to Distributed Systems: Goals of distributed system, Hardware and software concepts, Design issues.
Communication in Distributed Systems: Layered protocols, ATM networks, Client - Server model, Remote procedure call and Group
communication.

UNIT–V

Synchronization in Distributed Systems:
Clock synchronization, Mutual exclusion, E-tech algorithms, Bully algorithm, Ring algorithm, Atomic transactions
Deadlocks: Dead lock in distributed systems, Distributed dead lock prevention and distributed dead lock detection.

TEXT BOOKS

1. The design of the UNIX Operating Systems – Maurice J. Bach, 1986, PHI.
2. Distributed Operating System - Andrew. S. Tanenbaum, 1994, PHI.
3. The Complete reference LINUX – Richard Peterson, 4th Ed., McGraw – Hill.

REFERENCE BOOKS

1. Operating Systems: Internal and Design Principles - Stallings, 6th Ed., PE.
2. Modern Operating Systems, Andrew S Tanenbaum, 3rd Ed., PE.
3. Operating System Principles- Abraham Silberchatz, Peter B. Galvin, Greg Gagne, 7th Ed., John Wiley
4. UNIX User Guide – Ritchie & Yates.
5. UNIX Network Programming - W.Richard Stevens, 1998, PHI.

GOKARAJU RANGARAJU

INSTITUTE OF ENGINEERING AND TECHNOLOGY

EMBEDDED C LAB

M.Tech (ES) | I Year - I Semester

Course Code: GR17D5082 | L/T/P/C : 0/0/4/2

COURSE OBJECTIVES

- To impart the knowledge of AVR/ 8051 architecture&its programming
- To extract the features of microcontroller and interfacing with different peripherals.
- To understand the concept of Embedded C /arduino programming.
- To know the working Environment on arduino IDE/ Keil IDE. • To Develop an application with Atmel/8051 microcontroller in Embedded c.

COURSE OUTCOMES: After going through this course the student will be able to

- Familiarize with programming and interfacing microcontrollers to various devices using Arduino.
- Acquire the knowledge of Atmel/8051 microcontroller architecture & its programming.
- Work on Arduino Uno /8051 microcontroller based boards.
- Develop an application in Arduino IDE using Embedded C .
- Interface Atmel Microcontroller with different peripherals.
- Implement a wireless based appliance control.
- Define and Design a project on the exposure with AVR/8051.

Note:

- Minimum of 10 experiments have to be conducted.
- The following programs have to be tested on 89C51 Development board/equivalent using Embedded C Language on Keil IDE or Equivalent.

1. Program to toggle all the bits of Port P1 continuously with 250 mS delay.
2. Program to toggle only the bit P1.5 continuously with some delay. Use Timer 0, mode 1 to create delay.
3. Program to interface a switch and a buzzer to two different pins of a Port such that the buzzer should sound as long as the switch is pressed.
4. Program to interface LCD data pins to port P1 and display a message on it.
5. Program to interface keypad. Whenever a key is pressed, it should be displayed on LCD.
6. Program to interface seven segment display unit.
7. Program to transmit a message from Microcontroller to PC serially using RS232.
8. Program to receive a message from PC serially using RS232.
9. Program to get analog input from Temperature sensor and display the temperature value on PC Monitor. Program to interface Stepper Motor to rotate the motor in clockwise and anticlockwise directions
10. Program to Sort RTOS on to 89C51 development board.
11. Program to interface Elevator.

OPEN ELECTIVE - I

GOKARAJU RANGARAJU

INSTITUTE OF ENGINEERING AND TECHNOLOGY

E - COMMERCE AND APPLICATIONS
(Open Elective I)

M.Tech (CSE) | I Year - I Semester

Course Code: GR17D5178 | L/T/P/C :3/1/0/4

Course Objectives

- To understand the interest and opportunity of e-commerce
- To know and understand the critical success factors in implementing an ecommerce
- System
- To know how to plan and how to manage e-commerce solutions
- To have hands on, real-life experience with electronic commerce applications
- To analyze and understand the human, technological and business environment
- Associated with e-commerce

Course Outcomes: At the end of the course, the student will be able to

- Understand the trends in e-Commerce and the use of the Internet.(Level 2)
- Analyze, Understand and Comparethe principles of E-commerce and basics of World Wide Web.(Level 2&4)
- Analyze, Understandthe concept of electronic data interchange and its legal, social and technical aspects.(Level 2&4)
- Understandand Evaluate the security issues ssssover the web, the available solutions and future aspects of e-commerce security .(Level 2&5)
- Understanding and Validating the concept of E-banking, electronic payment system.(Level 2&5)
- Understand, Analyze and Comparethe capabilities and limitation of agents, Web based marketing and various security Issues. (Level 2&4)
- Understandingand Evaluation of online advertisements, website design issues and Creating a business transaction using an e commerce site.(Level 2,5 &6)

UNIT-I

INTRODUCTION Traditional commerce and E commerce – Internet and WWW – role of WWW – value chains – strategic business and Industry value chains – role of E commerce, advantages of E commerce, anatomy of e commerce applications.

UNIT-II

INFRASTRUCTURE FOR E COMMERCE Packet switched networks – TCP/IP protocol script – Internet utility programmes – SGML, HTML and XML – web client and servers – Web client/server architecture – intranet and extranets.

UNIT-III

WEB BASED TOOLS FOR E COMMERCE Web server – performance evaluation - web server software feature sets – web server software and tools – web protocol – search engines – intelligent agents –EC software – web hosting – cost analysis

UNIT- IV

SECURITY Computer security classification – copy right and Intellectual property – electronic commerce threats – protecting client computers – electronic payment systems and risks involved in it –electronic cash __ micro payment system– strategies for marketing – sales and promotion – cryptography –authentication.

UNIT-V

INTELLIGENT AGENTS Definition and capabilities – limitation of agents – security – web based marketing – search engines and Directory registration – online advertisements – Portables and info mechanics – website design issues.

TEXT BOOKS

1. Ravi Kalakota, " Electronic Commerce", Pearson Education,
2. Gary P Schneider "Electronic commerce", Thomson learning & James T Peny Cambridge USA, 2001.

REFERENCES BOOK

1. EfraimTurvanJ.Lee, David kug and chung, "Electronic commerce" Pearson Education Asia 2001.
2. Brenda Kienew E commerce Business Prentice Hall, 2001.
3. Manlyn Greenstein and Miklos "Electronic commerce" McGraw-Hill, 2002.

GOKARAJU RANGARAJU

INSTITUTE OF ENGINEERING AND TECHNOLOGY

ENTERPRISE RESOURCE PLANNING
(Open Elective-I)

M.Tech (IT) I Year - I Semester

Course Code: GR17D5179 L/T/P/C :3/1/0/4

PREREQUISITES

- Fundamentals of enterprise resource planning (ERP) systems concepts
- Importance of integrated information systems in an organization.

COURSE OBJECTIVES: The objective of the course is to provide the student

- Understanding of the basic concepts of ERP systems for manufacturing or service companies, and the differences among MRP, MRP II, and ERP systems
- Thinking in ERP systems: the principles of ERP systems, their major components, and the relationships among these components
- Capability to adapt in-depth knowledge of major ERP components, including material requirements planning, master production scheduling, and capacity requirements planning
- Understanding knowledge of typical ERP systems, and the advantages and limitations of implementing such systems
- Understanding the business process of an enterprise
- Grasp the activities of ERP project management cycle
- Understanding the emerging trends in ERP developments

COURSE OUTCOMES: At the end of the course the student will be able to

- Examine systematically the planning mechanisms in an enterprise, and identify all components in an ERP system and the relationships among the components
- Understand production planning in an ERP system, and systematicallydevelop plans for an enterprise
- Use methods to determine the correct purchasing quantity and right time to buy an item, and apply these methods to material management
- Understand the difficulties of a manufacturing execution system, select a suitable performance measure for different objectives, and apply priority rules to shop floor control
- Knowledge of ERP implementation cycle
- Awareness of core and extended modules of ERP
- Apply emerging trends in ERP

UNIT-I

Introduction: Overview – Benefits of ERP – ERP and Related Technologies – Business Process Reengineering – Data Warehousing – Data Mining – On–line Analytical Processing – Supply Chain Management.

UNIT-II

IMPLEMENTATION: Implementation Life Cycle – Implementation Methodology – Hidden Costs – Organizing Implementation – Vendors, Consultants and Users – Contracts – Project Management and Monitoring.

UNIT- III

BUSINESS MODULES: Business Modules in an ERP Package – Finance – Manufacturing – Human Resource –Plant Maintenance – Materials Management – Quality Management – Sales and Distribution.

UNIT- IV

ERP MARKET: ERP Market Place – SAP AG – PeopleSoft – Baan Company – JD Edwards World Solutions Company – Oracle Corporation – QAD – System Software Associates.

UNIT- V

ERP-Present and future : Turbo Charge the ERP System – EIA – ERP and E–Commerce – ERP and Internet – Future Directions in ERP.

TEXT BOOKS

1. Alexis Leon, “ERP Demystified”, Tata McGraw Hill, 1999.
2. Joseph A. Brady, Ellen F. Monk, Bret J. Wangner, “Concepts in Enterprise Resource Planning” , Thomson Learning, 2001.
3. Vinod Kumar Garg and N.K .Venkata Krishnan, “Enterprise Resource Planning – concepts and Planning”, Prentice Hall, 1998.
4. Jose Antonio Fernandz, “ The SAP R /3 Hand book”, Tata McGraw Hill

GOKARAJU RANGARAJU

INSTITUTE OF ENGINEERING AND TECHNOLOGY

MODERN CONTROL THEORY
(Open Elective-I)

M.Tech (EEE) I Year - I Semester

Course Code: GR17D5180 L/T/P/C :3/1/0/4

PREREQUISITE: Control Systems, Mathematics.

COURSE OBJECTIVES

- To familiarize students with the modelling of systems
- To familiarize the students with the state space analysis of dynamic systems and observe their controllability and Observability.
- To make students understand the concepts of describing function analysis of nonlinear systems and analyze the stability of the systems.
- To analyze the stability of the nonlinear systems.

COURSE OUTCOMES

- Ability to obtain the mathematical model of any system.
- Ability to obtain the state model for dynamic systems.
- Ability to analyze the controllability and Observability for various types of control systems.
- Ability to understand the various types of nonlinearity.
- Ability to analyze the stability of the nonlinear systems.
- Ability to synthesize the nonlinear systems.

UNIT-I

MATHEMATICAL PRELIMINARIES: Fields, Vectors, Vector Spaces — Linear combinations and Bases — Linear Transformations and Matrices — Scalar Product and Norms ,Eigenvalues, Eigen Vectors and a Canonical form representation of linear operators, The concept of state — State Equations for Dynamic systems, Time invariance and Linearity Non uniqueness of state model — State diagrams for Continuous-Time State models.

UNIT-II

STATE VARIABLE ANALYSIS: linear Continuous time models for Physical systems-- Existence and Uniqueness of Solutions to Continuous- time State Equations — Solutions of Linear Time Invariant Continuous-Time State Equations—State transition matrix and it's properties.

CONTROLLABILITY AND OBSERVABILITY-General concept of controllability— General concept of Observability—Controllability tests for Continuous-Time Invariant Systems ---
Observability tests for Continuous-Time Invariant Systems— Controllability and Observability of State Model in Jordan Canonical form— Controllability and Observability Canonical forms of State model.

UNIT- III

NON LINEAR SYSTEMS -I

Introduction to Non Linear Systems - Types of Non-Linearities-Saturation-Dead-Zone - Backlash Jump Phenomenon etc;— Singular Points-Introduction to Linearization of nonlinear systems, Properties of Non Linear systems-Describing function-describing function analysis of nonlinear systems-Stability analysis of Non-Linear systems through describing functions.

UNIT-IV

NON LINEAR SYSTEMS-II

Introduction to phase-plane analysis, Method of Isoclines for Constructing Trajectories, singular points, phase- plane analysis of nonlinear control systems.

UNIT-V

STABILITY ANALYSIS

Stability in the sense of Lyapunov, Lyapunovs stability and Lyapunov's instability theorems - StabilityAnalysis of the Linear continuous time invariant systems by Lyapunov second method — Generation of Lyapunov functions Variable gradient method — Krasooviski's method.

TEACHING METHODOLOGIES

1. White board
2. PPTs
3. Seminars

EXT BOOKS

1. Modern Control System Theory by M.Gopal — New Age International -1999
2. Modern Control Fngineering by Ogata:K — Prentice Hall – 1997

REFERENCE BOOK

1. Control Systems Engineering, N. S. Nise: 4th Ed., Wiley, 2004.Engineering, 4th Ed., Wiley, 2004.

GOKARAJU RANGARAJU

INSTITUTE OF ENGINEERING AND TECHNOLOGY

COMPUTER–ORIENTED NUMERICAL METHODS IN ENGINEERING
(Open Elective-I)

M.Tech (Civil) I Year - I Semester

Course Code: GR17D5181 L/T/P/C :3/1/0/4

COURSE OBJECTIVES

- To develop the skill of solving linear algebraic systems by direct and iteration methods.
- To illustrate advanced matrix techniques in the determination of Eigen values and Eigen vectors of square matrix.
- To analyze the performance of various interpolation technique and perform error analysis.
- To compare various numerical differentiation and integration techniques. •
- To explain the various techniques to study Initial and Boundary value problems in ODE.
- To solve a range of problems on applicable software.

COURSE OUT COMES: At the end of the course the student will be able to

- Solve linear algebraic system by direct and iteration methods.
- Apply the knowledge of Eigen values and Eigen vectors to some contents in engineering.
- Develop the skill of working with symmetric matrices in the study of Engineering problems.
- Apply the knowledge of interpolation and extrapolation of uniform and non uniform data to certain contents of Civil Engineering.
- Apply the knowledge of numerical differentiation and integration to some contents of Civil Engineering
- Learn grid based methods to solve Initial and Boundary value problems that arise in engineering problems.
- Develop the skill of solving computational problems using software.

UNIT-I

Solutions of linear equations: Direct method – Cramer's rule, Guass – Elimination method-Gauss Jordan elimination – Triangulation (LU Decomposition) method – Iterative methods Jacobi – Iteration method – Gauss – Siedel iteration, Successive over –relaxation method.
Eigen values and eigen vectors: Jacobi method for symmetric matrices- Given's method for symmetric matrices-Householder's method for symmetric matrices-Rutishauser method of arbitrary matrices –Power method.*Demonstration of solutions using open source software in Numerical Methods.

UNIT-II

Interpolation: Linear Interpolation - Higher order Interpolation - Lagrange Interpolation – Interpolating polynomials using finites differences- Hermite Interpolation -piece-wise and spline Interpolation.*Demonstration of solutions using open source software in Numerical methods.

UNIT - III

Finite Difference and their Applications: Introduction- Differentiation formulas by Interpolating parabolas – Backward and forward and central differences- Derivation of Differentiation formulae using Taylor series- Boundary conditions- Beam deflection – Solution of characteristic value problems- Richardson's extrapolation- Use of unevenly spaced pivotal points- Integration formulae by interpolating parabolas- Numerical solution to spatial differential equations. *Demonstration of solutions using open source software in Numerical Methods.

UNIT-IV

Numerical Differentiation: Difference methods based on undetermined coefficients- optimum choice of step length– Partial differentiation. Numerical Integration: Method based on interpolation-method based on undetermined coefficient – Gauss – Lagrange interpolation method- Radaua integration method- composite integration method – Double integration using Trapezoidal and Simpson's method.*Demonstration of solutions using open source software in Numerical Methods.

UNIT-V

Ordinary Differential Equation: Euler's method – Backward Euler method – Mid point method – single step method, Taylor's series method- Boundary value problems-case studies. *Demonstration of solutions using open source software in Numerical Methods.

***NOTE:** Demonstration of solutions using open source software in Numerical Methods only for the knowledge of students to apply in their Project Works. Not for examination.

TEXT BOOKS

1. M.K.Jain-S.R.K.Iyengar, R.K.Jain Numerical methods for scientific and engineering computations, Willey Eastern Limited, 1987
2. S.S.Shastry, Numerical methods.
3. Curtis I.Gerala, Applied numerical analysis, Addisson Wasley published campus.

REFERENCES BOOKS

1. C.Chopra, Raymond P.Canal, Numerical methods for Engineers Stevan, Mc. Graw Hill book Company, 4th edition, 2002.
2. C.Xavier, C Language and Numerical methods, New age international publisher, 2003.
3. Dr. M.Shanta Kumar, Computer based numerical analysis, Khanna Book publishers, New Delhi.

GOKARAJU RANGARAJU

INSTITUTE OF ENGINEERING AND TECHNOLOGY

ADVANCED COMPUTER ARCHITECTURE
(Open Elective-I)

M.Tech (ECE) I Year - I Semester

Course Code: GR17D5182 L/T/P/C :3/1/0/4

COURSE OBJECTIVES

- To learn how to build the best processor/computing system understanding the underlying tradeoffs and ramifications.
- To identify and analyze the attributes of computer architecture design with recent trend technology.
- To identify the techniques to improve the speed and performance of computers – Parallelism in Instruction level – Hardware approaches - pipelining,dynamic scheduling, superscalar processors, and multiple issue of instructions.
- To implement the design aspects and categorize various issues , causes and hazards due to parallelisms.
- To examine and compare the performance with benchmark standards.
- To understand the framework for evaluating design decisions in terms of application requirements and performance measurements.
- To learn the design and analysis of complex and high performance multiprocessors and supporting subsystems from the quantitative aspect.

COURSE OUTCOMES: After going through this course the student will be able to

- An ability to discuss the organisation of computer-based systems and how a range of design choices are influenced by applications.
- An ability to understand the components and operation of a memory hierarchy and the range of performance issues influencing its design.
- An ability to interpret the organisation and operation of current generation parallel computer systems, including multiprocessor and multicore systems.
- An ability to understand the various techniques to enhance a processors ability to exploit instruction-level parallelism (ILP), and its challenges.
- An ability to know the classes of computers, and new trends and developments in computer architecture.
- An ability to develop the applications for high performance computing systems.
- An ability to undertake performance comparisions of modern and high performance computers.

UNIT -I

Fundamentals of Computer Design: Fundamentals of Computer design, Changing faces of computing and task of computer designer, Technology trends, Cost price and their trends, measuring and reporting performance, Quantitative principles of computer design, Amdahl's law.

Instruction set principles and examples- Introduction, classifying instruction set- memory addressing type and size of operands, Operations in the instruction set.

UNIT-II

Pipelines: Introduction, basic RISC instruction set, Simple implementation of RISC instruction set, Classic five stage pipe lined RISC processor, Basic performance issues in pipelining, Pipeline hazards, Reducing pipeline branch penalties.

Memory Hierarchy Design: Introduction, review of ABC of cache, Cache performance, Reducing cache miss penalty, Virtual memory.

UNIT-III

Instruction Level Parallelism (ILP) - The Hardware Approach: Instruction-Level parallelism, Dynamic scheduling, Dynamic scheduling using Tomasulo's approach, Branch prediction, High performance instruction delivery- Hardware based speculation.

ILP Software Approach:

Basic compiler level techniques, Static branch prediction, VLIW approach, Exploiting ILP, Parallelism at compile time, Cross cutting issues - Hardware verses Software.

UNIT-IV

Multi Processors and Thread Level Parallelism: Multi Processors and Thread level Parallelism-Introduction, Characteristics of application domain, Systematic shared memory architecture, Distributed shared – Memory architecture, Synchronization.

UNIT-V

Inter Connection and Networks: Introduction, Interconnection network media, Practical issues in interconnecting networks, Examples of inter connection, Cluster, Designing of clusters.
Intel Architecture: Intel IA-64 ILP in embedded and mobile markets Fallacies and pit falls.

TEXT BOOKS

1. John L. Hennessy, David A. Patterson - Computer Architecture: A Quantitative Approach, 3rd Edition, an Imprint of Elsevier.

REFERENCE BOOKS

1. John P. Shen and Miikko H. Lipasti -, Modern Processor Design : Fundamentals of Super Scalar Processors
2. Computer Architecture and Parallel Processing - Kai Hwang, Faye A.Brigs., MC Graw Hill.

GOKARAJU RANGARAJU

INSTITUTE OF ENGINEERING AND TECHNOLOGY

OPERATIONS RESEARCH
(Open Elective-I)

Mtech(ME) I Year - I Semester

Course Code: GR17D5183 L/T/P/C :3/1/0/4

COURSE OBJECTIVES: The Objective of this course is to provide

- Analysis of quantitative methods and techniques for effective Decision–making.
- Constructing models that are used in solving business decision problems.
- Introduce the students to the use of basic methodology for the solution of linear programs and integer programs.
- Introduce the students to methods for solving large-scale transportation and assignment problems.
- Illustrate how sequencing is carried out in assigning jobs to machines
- Understand the concept of Inventory and apply different models in optimizing the same.
- Apply PERT/CPM: [Project scheduling and allocation of resources] to schedule and control construction of dams, bridges, roads etc. in an optimal way.

COURSE OUTCOMES: At the end of the course, the student will be able to:

- Apply various linear programming techniques for optimal allocation of limited resources such as machine, materials and money
- Solve transportation problems to minimize cost and understand the principles of assignment of jobs and recruitment polices.
- Solve game theory problems.
- Solve problems of inventory and develop proper inventory policies.
- Apply PERT/CPM: [Project scheduling and allocation of resources] to schedule and control construction of dams, bridges, roads etc in a optimal way.
- Solve sequencing problems.
- Develop optimum replacement policy

UNIT-I

Introduction: Definition and scope of operations research(OR),ORmodel, solving the O**R** model, art of modeling, phases of OR study.

Linear Programming:

Two variable Linear Programming model and Graphical method of solution, Simplex method, Dual Simplex method, special cases of Linear Programming, duality, sensitivity analysis.

UNIT-II

Transportation Problems: Types of transportation problems, mathematical models, transportation algorithms

Assignment: Allocation and assignment problems and models, processing of job through machines.

UNIT-III

Network Techniques: Shortest path model, minimum spanning Tree Problem, Max-Flow problem and Min-cost problem.
Project Management: Phases of project management, guidelines for network construction, CPM and PERT.

UNIT-IV

Theory of Games: Rectangular games, Min-max theorem, graphical solution of 2xnormx2 games, game with mixed strategies, reduction to linear programming model.
Quality Systems: Elements of Queuing model, generalized Poisson queuing model.

UNIT-V

Inventory Control: Models of inventory, operation of inventory system, quantity discount.
Replacement models: Equipments that deteriorate with time, equipments that fail with time.

TEXT/ REFERENCE BOOKS:

1. Wayne L. Winston,"OperationsResearch", Thomson Learning, 2003.
2. Hamdy H. Taha, "Operations Research - An Introduction", Pearson Education, 2003.
3. R. Panneer Seevam, "Operations Research", PHI Learning, 2008.
4. V. K. Khanna, "Total Quality Management", New Age International, 2008.

TEACHING METHODOLOGY

1. Lecture is delivered on blackboard, preparing OHP sheets and by preparing Power point presentations.
2. Seminars are conducted on new technologies related to subject.
3. Assignments are given.
4. Group discussions are conducted on familiar topics related to subject.
5. Industrial visits for practical exposure to understand and explore things.

II- SEMESTER

GOKARAJU RANGARAJU

INSTITUTE OF ENGINEERING AND TECHNOLOGY

DIGITAL SIGNAL PROCESSORS AND ARCHITECTURES

M.Tech (ES) I Year - II Semester

Course Code: GR17D5084 L/T/P/C :3/1/0/4

COURSE OBJECTIVES

- To provide sound foundation of digital signal processing (DSP) architectures for designing efficient VLSI architectures for DSP systems.
- To analyze general purpose digital signal processors.
- To understand pipelining, parallel processing and retiming.
- To illustrate the features of on-chip peripheral devices and its interfacing along with its programming details.
- To analyze DSP architectures.

COURSE OUTCOMES: After going through this course the student will be able to

- An ability to design analog and digital filters for signal-processing applications.
- An ability to recognize the fundamentals of fixed and floating point architectures of various DSPs.
- An ability to learn the architecture details and instruction sets of fixed and floating point DSPs.
- An ability to Infer about the control instructions, interrupts, and pipeline operations.
- An ability to analyze and learn to implement the signal processing algorithms in DSPs.
- An ability to learn the DSP programming tools and use them for applications.
- An ability to design and implement signal processing modules in DSPs.

UNIT –I

Introduction to Digital Signal Processing: Introduction, a Digital signal-processing system, the sampling process, discrete time sequences. Discrete Fourier Transform (DFT) and Fast Fourier Transform (FFT), Linear time-invariant systems, Digital filters, Decimation and interpolation.

Computational Accuracy in DSP Implementations:

Number formats for signals and coefficients in DSP systems, Dynamic Range and Precision, Sources of error in DSP implementations, A/D Conversion errors, DSP Computational errors, D/A Conversion Errors, Compensating filter.

UNIT –II

Architectures for Programmable DSP Devices: Basic Architectural features, DSP Computational Building Blocks, Bus Architecture and Memory, Data Addressing Capabilities, Address Generation UNIT, Programmability and Program Execution, Speed Issues, Features for External interfacing.

UNIT -III

Programmable Digital Signal Processors: Commercial Digital signal-processing Devices, Data Addressing modes of TMS320C54XX DSPs, Data Addressing modes of TMS320C54XX Processors, Memory space of TMS320C54XX Processors, Program Control, TMS320C54XX Instructions and Programming, On-Chip Peripherals, Interrupts of TMS320C54XX Processors, Pipeline Operation of TMS320C54XX Processors.

UNIT –IV

Analog Devices Family of DSP Devices: Analog Devices Family of DSP Devices – ALU and MAC block diagram, Shifter Instruction, Base Architecture of ADSP 2100, ADSP-2181 high performance Processor. Introduction to Black fin Processor - The Black fin Processor, Introduction to Micro Signal Architecture, Overview of Hardware Processing Units and Register files, Address Arithmetic Unit, Control Unit, Bus Architecture and Memory, Basic Peripherals.

UNIT –V

Interfacing Memory and I/O Peripherals to Programmable DSP Devices: Memory space organization, External bus interfacing signals, Memory interface, Parallel I/O interface, Programmed I/O, Interrupts and I/O, Direct memory access (DMA).

TEXT BOOKS

1. Digital Signal Processing – Avtar Singh and S. Srinivasan, Thomson Publications, 2004.
2. A Practical Approach To Digital Signal Processing - K Padmanabhan, R. Vijayarajeswaran, Ananthi. S, New Age International, 2006/2009
3. Embedded Signal Processing with the Micro Signal Architecture: Woon-Seng Gan, Sen M.Kuo, Wiley-IEEE Press, 2007

REFERENCE BOOKS

1. Digital Signal Processors, Architecture, Programming and Applications – B. Venkataramani and M. Bhaskar, 2002, TMH.
2. Digital Signal Processing – Jonatham Stein, 2005, John Wiley.

GOKARAJU RANGARAJU

INSTITUTE OF ENGINEERING AND TECHNOLOGY

EMBEDDED NETWORKING

M.Tech (ES) I Year - II Semester

Course Code: GR17D5085 L/T/P/C :3/1/0/4

COURSE OBJECTIVES

- To study various Embedded communication protocols.
- To learn USB and CAN bus protocols.
- To know the basics of Ethernet module.
- To understand the concept of Embedded webserver.
- To familiarize about wireless sensor networks.

COURSE OUTCOMES: After going through this course the student will be able to

- Differentiate serial and parallel communication protocols.
- Design and develop an application using USB and CAN Protocols
- Demonstrate working principle of Ethernet module.
- Write a HTML code for creating webpages.
- Develop an application for serving webpages with dynamic data.
- Interface different devices in a wireless configuration.
- Carry out energy-efficient routing in wireless embedded networking.

UNIT –I

Embedded Communication Protocols: Embedded Networking: Introduction – Serial/Parallel Communication – Serial communication protocols -RS232 standard – RS485 – Synchronous Serial Protocols -Serial Peripheral Interface (SPI) – Inter Integrated Circuits (I2C) – PC Parallel port programming - ISA/PCI Bus protocols – Firewire.

UNIT –II

USB and CAN Bus: USB bus – Introduction – Speed Identification on the bus – USB States – USB bus communication: Packets –Data flow types –Enumeration –Descriptors –PIC 18 Microcontroller USB Interface – C Programs –CAN Bus – Introduction - Frames –Bit stuffing – Types of errors –Nominal Bit Timing – PIC microcontroller CAN Interface –A simple application with CAN.

UNIT –III

Ethernet Basics: Elements of a network – Inside Ethernet – Building a Network: Hardware options – Cables, Connections and network speed – Design choices: Selecting components –Ethernet Controllers –Using the internet in local and internet communications – Inside the Internet protocol.

UNIT –IV

Embedded Ethernet: Exchanging messages using UDP and TCP – Serving web pages with Dynamic Data – Serving web pages that respond to user Input – Email for Embedded Systems – Using FTP – Keeping Devices and Network secure.

UNIT –V

Wireless Embedded Networking: Wireless sensor networks – Introduction – Applications – Network Topology – Localization –Time Synchronization - Energy efficient MAC protocols –SMAC – Energy efficient and robust routing –Data Centric routing.

TEXT BOOKS

1. Embedded Systems Design: A Unified Hardware/Software Introduction - Frank Vahid, Tony Givargis, John & Wiley Publications, 2002
2. Parallel Port Complete: Programming, interfacing and using the PCs parallel printer port - Jan Axelson, Penram Publications, 1996.

REFERENCE BOOKS

1. Advanced PIC microcontroller projects in C: from USB to RTOS with the PIC18F series - Dogan Ibrahim, Elsevier 2008.
2. Embedded Ethernet and Internet Complete - Jan Axelson, Penram publications, 2003.
3. Networking Wireless Sensors - BhaskarKrishnamachari, Cambridge press 2005.

GOKARAJU RANGARAJU

INSTITUTE OF ENGINEERING AND TECHNOLOGY

CPLD AND FPGA ARCHITECTURES AND APPLICATIONS

M.Tech (ES) I Year - II Semester

Course Code: GR17D5086 L/T/P/C :3/1/0/4

COURSE OBJECTIVES

- To understand the concept of Programmable Logic Device architectures and technologies.
- Underlying FPGA architectures and technologies in detail.
- To understand the difference between CPLDs and FPGAs
- To provide knowledge about SRAM Programmable FPGA Device architecture.
- To comprehend knowledge about Anti-Fuse Programmable FPGA Device architecture.
- To furnish knowledge about various applications of FPGA.
- To provide knowledge about FPGA based case studies.

COURSE OUTCOMES: After going through this course the student will be able to

- To know the concept of programmable architectures.
- Perceiving CPLD and FPGA technologies
- Study and compare the different architectures of CPLDs and FPGAs
- An ability to know the SRAM Technology based FPGAs
- An ability to know the Anti-Fuse Technology based FPGAs
- Design and impose applications using FPGAs.
- Construct a digital system using FPGA.

UNIT-I

Introduction to Programmable Logic Devices: Introduction, Simple Programmable Logic Devices – Read Only Memories, Programmable Logic Arrays, Programmable Array Logic, Programmable Logic Devices/Generic Array Logic; Complex Programmable Logic Devices – Architecture of Xilinx Cool Runner XCR3064XL CPLD, CPLD Implementation of a Parallel Adder with Accumulation.

UNIT-II

Field Programmable Gate Arrays: Organization of FPGAs, FPGA Programming Technologies, Programmable Logic Block Architectures, Programmable Interconnects, Programmable I/O blocks in FPGAs, Dedicated Specialized Components of FPGAs, Applications of FPGAs.

UNIT -III

SRAM Programmable FPGAs: Introduction, Programming Technology, Device Architecture, The Xilinx XC2000, XC3000 and XC4000 Architectures.

UNIT -IV

Anti-Fuse Programmed FPGAs: Introduction, Programming Technology, Device Architecture, TheActel ACT1, ACT2 and ACT3 Architectures.

UNIT -V

Design Applications: General Design Issues, Counter Examples, A Fast Video Controller, A Position Tracker for a Robot Manipulator, A Fast DMA Controller, Designing Counters with ACT devices, Designing Adders and Accumulators with the ACT Architecture.

TEXT BOOKS

1. Field Programmable Gate Array Technology - Stephen M. Trimberger, Springer International Edition.
2. Digital Systems Design - Charles H. Roth Jr, Lizy Kurian John, Cengage Learning.

REFERENCE BOOKS

1. Field Programmable Gate Arrays - John V. Oldfield, Richard C. Dorf, Wiley India.
2. Digital Design Using Field Programmable Gate Arrays - Pak K. Chan/SamihaMourad, Pearson Low Price Edition.
3. Digital Systems Design with FPGAs and CPLDs - Ian Grout, Elsevier, Newnes.
4. FPGA based System Design - Wayne Wolf, Prentice Hall Modern Semiconductor Design Series.

GOKARAJU RANGARAJU
INSTITUTE OF ENGINEERING AND TECHNOLOGY

SENSORS AND ACTUATORS
(ELECTIVE–III)

M.Tech (ES) I Year - II Semester
Course Code: GR17D5087 L/T/P/C :3/1/0/4

COURSE OBJECTIVES

- Describe the criteria for selecting a sensor for a particular measurement.
- Relate some basic principles and techniques of micro sensors and actuators.
- Determine characteristics of various types of mechanical sensors.
- Interpret physical principles applied in sensors and actuators.
- Identify various types of sensors including thermal, mechanical, electrical, electro mechanical and optical sensors.
- Classify of imminent Sensors and Actuators.
- Apply the acquired knowledge to specific Sensors and Actuators related problems and projects at work.

COURSE OUTCOMES: After going through this course the student will be able to

- Relate about the working principles and architecture of a large number of sensors and their elements.
- Classify the use sensors and equipment for measuring mechanical quantities and temperature.
- Apply the architecture and working principles of the most common electrical motor types.
- Identify and discriminate various electrical drives and actuators.
- Analyze and interpret in an active way with the specialists in these areas.
- Identify the forthcoming Sensors and Actuators.
- Take advanced course in this area.

UNIT -I

Sensors / Transducers: Principles – Classification – Parameters – Characteristics – Environmental Parameters (EP) – Characterization

Mechanical and Electromechanical Sensors: Introduction – Resistive Potentiometer – Strain Gauge – Resistance Strain Gauge – Semiconductor Strain Gauges -Inductive Sensors: Sensitivity and Linearity of the Sensor –Types-Capacitive Sensors:– Electrostatic Transducer– Force/Stress Sensors Using Quartz Resonators – Ultrasonic Sensors

UNIT –II

Thermal Sensors: Introduction – Gas thermometric Sensors – Thermal Expansion Type Thermometric Sensors – Acoustic Temperature Sensor – Dielectric Constant and Refractive Index thermosensors – Helium Low Temperature Thermometer – Nuclear Thermometer – Magnetic Thermometer – Resistance Change Type Thermometric Sensors –Thermoemf Sensors– Junction

Semiconductor Types– Thermal Radiation Sensors –Quartz Crystal Thermoelectric Sensors – NQR Thermometry – Spectroscopic Thermometry – Noise Thermometry – Heat Flux Sensors Magnetic sensors: Introduction – Sensors and the Principles Behind – Magneto-resistive Sensors –Anisotropic Magnetoresistive Sensing – Semiconductor Magnetoresistors– Hall Effect and Sensors –Inductance and Eddy Current Sensors– Angular/Rotary Movement Transducers – Synchros –Synchro-resolvers - Eddy Current Sensors – Electromagnetic Flowmeter – Switching Magnetic Sensors SQUID Sensors

UNIT -III

Radiation Sensors: Introduction – Basic Characteristics – Types of Photosensistors/Photo detectors– X-ray and Nuclear Radiation Sensors– Fiber Optic Sensors
Electro analytical Sensors: Introduction – The Electrochemical Cell – The Cell Potential – Standard Hydrogen Electrode (SHE) – Liquid Junction and Other Potentials – Polarization – Concentration Polarization-– Reference Electrodes - Sensor Electrodes – Electro ceramics in Gas Media .

UNIT -IV

Smart Sensors: Introduction – Primary Sensors – Excitation – Amplification – Filters – Converters –Compensation– Information Coding/Processing - Data Communication – Standards for Smart Sensor Interface – The Automation
Sensors–Applications: Introduction – On-board Automobile Sensors (Automotive Sensors)– Home Appliance Sensors – Aerospace Sensors –– Sensors for Manufacturing –Sensors for environmental Monitoring

UNIT -V

Actuators: Pneumatic and Hydraulic Actuation Systems- Actuation systems – Pneumatic and hydraulic systems - Directional Control valves – Presure control valves – Cylinders - Servo and proportional control valves – Process control valves – Rotary actuators Mechanical Actuation Systems- Types of motion – Kinematic chains – Cams – Gears – Ratchet and pawl – Belt and chain drives – Bearings – Mechanical aspects of motor selection Electrical Actuation Systems- Electrical systems -Mechanical switches – Solid-state switches
Solenoids – D.C. Motors – A.C. motors – Stepper motors

TEXT BOOKS

1. D. Patranabis – “Sensors and Transducers” –PHI Learning Private Limited.
2. W. Bolton – “Mechatronics” –Pearson Education Limited.

REFERENCE BOOKS

1. Sensors and Actuators – D. Patranabis – 2nd Ed., PHI, 2013.

GOKARAJU RANGARAJU

INSTITUTE OF ENGINEERING AND TECHNOLOGY

WIRELESS COMMUNICATIONS AND NETWORKS (ELECTIVE–III)

M.Tech (ES) I Year - II Semester
Course Code: GR17D5088 L/T/P/C :3/1/0/4

COURSE OBJECTIVES:

- To study the cellular system fundamentals, like frequency re-use, Handoff and interferences.
- To study different indoor propagation models.
- To study different outdoor propagation models.
- To study small-scale and large-scale fading.
- To study frequency-selective and frequency-flat fading.
- To study equalisation fundamental and various equalisers.
- To study diversity fundamentals and various diversity schemes.
- To study various standards.

COURSE OUTCOMES: After going through this course the student will be able to

- The student will be able to apply the concepts of frequency re-use, Handoff and interferences in design of cellular system.
- The student will be able to predict the signal strength under indoor and outdoor propagation conditions.
- The student will be able to involve in channel sounding system designs,
- The student will be able to involve in design of equalisers.
- The student will be able to involve in design of various diversity schemes.
- The student will be able to involve in design of IEEE 802.11 network.
- The student will be able to involve in design of IEEE 802.16 network.

UNIT -I

The Cellular Concept-System Design Fundamentals: Introduction, Frequency Reuse, Channel Assignment Strategies, Handoff Strategies- Prioritizing Handoffs, Practical Handoff Considerations, Interference and system capacity – Co channel Interference and system capacity, Channel planning for Wireless Systems, Adjacent Channel interference , Power Control for Reducing interference, Trunking and Grade of Service, Improving Coverage & Capacity in Cellular Systems- Cell Splitting, Sectoring .

UNIT –II

Mobile Radio Propagation: Large-Scale Path Loss: Introduction to Radio Wave Propagation, Free Space Propagation Model, Relating Power to Electric Field, The Three Basic Propagation Mechanisms, Reflection-Reflection from Dielectrics, Brewster Angle, Reflection from prefect conductors, Ground Reflection (Two-Ray) Model, Diffraction-Fresnel Zone Geometry, Knife-edge

Diffraction Model, Multiple knife-edge Diffraction, Scattering, Outdoor Propagation Models-Longley- Ryce Model, Okumura Model, Hata Model, PCS Extension to Hata Model, Walfisch and Bertoni Model, Wideband PCS Microcell Model, Indoor Propagation Models-Partition losses (Same Floor), Partition losses between Floors, Log-distance path loss model, Ericsson Multiple Breakpoint Model, Attenuation Factor Model, Signal penetration into buildings, Ray Tracing and Site Specific Modeling.

UNIT –III:

Mobile Radio Propagation: Small –Scale Fading and Multipath: Small Scale Multipath propagation-Factors influencing small scale fading, Doppler shift, Impulse Response Model of a multipath channel- Relationship between Bandwidth and Received power, Small-Scale Multipath Measurements-Direct RF Pulse System, Spread Spectrum Sliding Correlator Channel Sounding, Frequency Domain Channels Sounding, Parameters of Mobile Multipath Channels-Time Dispersion Parameters, Coherence Bandwidth, Doppler Spread and Coherence Time, Types of Small-Scale Fading-Fading effects Due to Multipath Time Delay Spread, Flat fading, Frequency selective fading, Fading effects Due to Doppler Spread-Fast fading, slow fading, Statistical Models for multipath Fading Channels-Clarke's model for flat fading, spectral shape due to Doppler spread in Clarke's model, Simulation of Clarke and Gans Fading Model, Level crossing and fading statistics, Two-ray Rayleigh Fading Model.

UNIT -IV

Equalization and Diversity: Introduction, Fundamentals of Equalization, Training A Generic Adaptive Equalizer, Equalizers in a communication Receiver, Linear Equalizers, Non linear Equalization-Decision Feedback Equalization (DFE), Maximum Likelihood Sequence Estimation (MLSE) Equalizer, Algorithms for adaptive equalization-Zero Forcing Algorithm, Least Mean Square Algorithm, Recursive least squares algorithm. Diversity Techniques-Derivation of selection Diversity improvement, Derivation of Maximal Ratio Combining improvement, Practical Space Diversity Consideration-Selection Diversity, Feedback or Scanning Diversity, Maximal Ratio Combining, Equal Gain Combining, Polarization Diversity, Frequency Diversity, Time Diversity, RAKE Receiver.

UNIT-V

Wireless Networks: Introduction to wireless Networks, Advantages and disadvantages of Wireless Local Area Networks, WLAN Topologies, WLAN Standard IEEE 802.11,IEEE 802.11 Medium Access Control, Comparision of IEEE 802.11 a,b,g and n standards, IEEE 802.16 and its enhancements, Wireless PANs, Hiper Lan, WLL.

TEXT BOOKS

1. Wireless Communications, Principles, Practice – Theodore, S. Rappaport, 2nd Ed., 2002, PHI.
2. Wireless Communications-Andrea Goldsmith, 2005 Cambridge University Press.
3. Mobile Cellular Communication – GottapuSasibhushana Rao, Pearson Education, 2012.

REFERENCE BOOKS

1. Principles of Wireless Networks – KavehPahLaven and P. Krishna Murthy, 2002, PE
2. Wireless Digital Communications – KamiloFeher, 1999, PHI.
3. Wireless Communication and Networking – William Stallings, 2003, PHI.
4. Wireless Communication – UpenDalal, Oxford Univ. Press
5. Wireless Communications and Networking – Vijay K. Gary, Elsevier.

GOKARAJU RANGARAJU

INSTITUTE OF ENGINEERING AND TECHNOLOGY

NETWORK SECURITY AND CRYPTOGRAPHY

(ELECTIVE – III)

M.Tech (ES) I Year - II Semester
Course Code: GR17D5089 L/T/P/C :3/1/0/4

COURSE OBJECTIVE

- To provide deeper understanding into cryptography, its application to network security, threats/vulnerabilities to networks and countermeasures.
- To study various approaches to Encryption techniques, strengths of Traffic Confidentiality, Message Authentication Codes.
- To know Digital Signature Standard and provide solutions for their issues.
- To be familiar with cryptographic techniques for secure (confidential) communication of two parties over an insecure (public) channel; verification of the authenticity of the source of a message.

COURSE OUTCOME: After going through this course the student will be able to

- To outline the different OSI layers and their functionalities.
- To impart knowledge on Encryption techniques, Design Principles and Modes of Operation.
- To design a security solution for a given application
- To understand the Key Management techniques and Number Theory.
- To create an understanding of Authentication functions the manner in which Message Authentication Codes and Hash Functions works.
- To examine the issues and structure of Authentication Service and Electronic Mail Security
- To provide familiarity in Intrusion detection and Firewall Design Principles.
- To Generate and distribute a PGP key pair and use the PGP package to send an encrypted e-mail message

UNIT –I

Introduction: Attacks, Services and Mechanisms, Security attacks, Security services, A Model for Internetwork security.Classical Techniques: Conventional Encryption model, Steganography, Classical Encryption Techniques.

UNIT –II

Modern Techniques: Simplified DES, Block Cipher Principles, Data Encryption standard, Strength of DES, Differential and Linear Cryptanalysis, Block Cipher Design Principles and Modes of operations.

Algorithms: Triple DES, International Data Encryption algorithm, Blowfish, RC5, CAST-128, RC2, Characteristics of Advanced Symmetric block cifers.

Conventional Encryption: Placement of Encryption function, Traffic confidentiality, Key distribution, Random Number Generation.

Public Key Cryptography: Principles, RSA Algorithm, Key Management, Diffie-Hellman Key exchange, Elliptic Curve Cryptography.

UNIT –III

Number Theory: Prime and Relatively prime numbers, Modular arithmetic, Fermat's and Euler's theorems, Testing for primality, Euclid's Algorithm, the Chinese remainder theorem, Discrete logarithms.

Message authentication and Hash Functions: Authentication requirements and functions, Message Authentication, Hash functions, Security of Hash functions and MACs.

UNIT –IV

Hash and Mac Algorithms: MD File, Message digest Algorithm, Secure Hash Algorithm, RIPEMD-160, HMAC. Digital signatures and Authentication Protocols: Digital signatures, Authentication Protocols, Digital signature standards.

Authentication Applications: Kerberos, X.509 directory Authentication service.Electronic Mail Security: Pretty Good Privacy, S/MIME.

UNIT –V

IP Security: Overview, Architecture, Authentication, Encapsulating Security Payload, Combining security Associations, Key Management.

Web Security: Web Security requirements, Secure sockets layer and Transport layer security, Secure Electronic Transaction.

Intruders,

Viruses and Worms: Intruders, Viruses and Related threats.

Fire Walls: Fire wall Design Principles, Trusted systems.

TEXT BOOKS

1. Cryptography and Network Security: Principles and Practice - William Stallings, Pearson Education.
2. Network Security Essentials (Applications and Standards) by William Stallings Pearson Education.

REFERENCE BOOKS

1. Fundamentals of Network Security by Eric Maiwald (Dreamtech press)
2. Network Security - Private Communication in a Public World by Charlie Kaufman, Radia Perlman and Mike Speciner, Pearson/PHI.

GOKARAJU RANGARAJU

INSTITUTE OF ENGINEERING AND TECHNOLOGY

MULTI MEDIA SIGNAL CODING
(ELECTIVE -IV)

M.Tech (ES) I Year - II Semester

Course Code: GR17D5090 L/T/P/C :3/1/0/4

COURSE OBJECTIVES

- To introduce the fundamental principles and techniques in multimedia signal processing and Compression
- Overview of current multimedia standards and technologies
- To understand and differentiate text, image, video & audio
- understand the basics of analog and digital video: video representation and transmission
- analyzeanalog and digital video signals and systems
- know the fundamental video processing techniques
- acquire the basic skill of designing video compression
- familiarize himself/herself with video compression standards
- Brief description of future technologies

COURSE OUTCOMES: After going through this course the student will be able to

- Understand the fundamentals behind multimedia signal processing and compression
- Understand the basic principles behind existing multimedia compression and communication
- differentiate multimedia and non-multimedia
- differentiate text, image, video &audio
- design and develop multimedia systems according to the requirements of multimedia applications
- understand different compression principles, compression techniques, multimedia compression standards
- program multimedia data and be able to design and implement media applications
- Understand future multimedia technologies
- Apply the acquired knowledge to specific multimedia related problems and projects at work

UNIT -I

Introduction to Multimedia: Multimedia, World Wide Web, Overview of Multimedia Tools, Multimedia Authoring, Graphics/ Image Data Types, and File Formats.

Color in Image and Video: Color Science – Image Formation, Camera Systems, Gamma Correction, Color Matching Functions, CIE Chromaticity Diagram, Color Monitor Specifications, Outof- Gamut Colors, White Point Correction, XYZ to RGB Transform, Transform with Gamma Correction, L*A*B* Color Model. Color Models in Images – RGB Color Model for CRT Displays, Subtractive Color: CMY Color Model, Transformation from RGB to CMY, Under Color Removal:

CMYK System, Printer Gamuts, Color Models in Video – Video Color Transforms, YUV Color Model, YIQ Color Model, YcbcrColor Model.

UNIT -II

Video Concepts: Types of Video Signals, Analog Video, Digital Video.
Audio Concepts: Digitization of Sound, Quantization and Transmission of Audio.

UNIT -III

Compression Algorithms: Lossless Compression Algorithms: Run Length Coding, Variable Length Coding, Arithmetic Coding, Lossless JPEG, Image Compression.
Lossy Image Compression Algorithms: Transform Coding: KLT And DCT Coding, Wavelet Based Coding.
Image Compression Standards: JPEG and JPEG2000.

UNIT -IV

Video Compression Techniques: Introduction to Video Compression, Video Compression Based on Motion Compensation, Search for Motion Vectors, H.261- Intra-Frame and Inter-Frame Coding, Quantization, Encoder and Decoder, Overview of MPEG1 and MPEG2.

UNIT -V

Audio Compression Techniques: ADPCM in Speech Coding, G.726 ADPCM, Vocoders – Phase Insensitivity, Channel Vocoder, Formant Vocoder, Linear Predictive Coding, CELP, Hybrid Excitation Vocoders, MPEG Audio – MPEG Layers, MPEG Audio Strategy, MPEG Audio Compression Algorithms, MPEG-2 AAC, MPEG-4 Audio.

TEXT BOOKS

1. Fundamentals of Multimedia – Ze- Nian Li, Mark S. Drew, PHI, 2010.
2. Multimedia Signals & Systems – Mrinal Kr. Mandal Springer International Edition 1st Edition,2009

REFERENCE BOOKS

1. Multimedia Communication Systems – Techniques, Stds&Netwroks K.R. Rao, Zorans. Bojkoric, DragoradA.Milovanovic, 1st Edition, 2002.
2. Fundamentals of Multimedia Ze- Nian Li, Mark S.Drew, Pearson Education (LPE), 1st Edition, 2009.
3. Multimedia Systems John F. KoegelBufond Pearson Education (LPE), 1st Edition, 2003.
4. Digital Video Processing – A. Murat Tekalp, PHI, 1996.

GOKARAJU RANGARAJU

INSTITUTE OF ENGINEERING AND TECHNOLOGY

SYSTEM ON CHIP ARCHITECTURE
(ELECTIVE -IV)

M.Tech (ES) I Year - II Semester

Course Code: GR17D5091 L/T/P/C :3/1/0/4

COURSE OBJECTIVES

- To describe the system design approach with respect to the hardware and software
- To apply the techniques for reducing the delays in program execution
- To categorize and compare different processor types for their selection into a System on Chip.
- To compare different memory designs and their purposes
- To interpret the architectures and applications of various buses.
- To analyze and choose from different reconfigurable devices for a system on chip.
- To interpret the standard algorithms like AES.

COURSE OUTCOMES: After going through this course the student will be able to

- Students will be able to summarize all the components required for system design.
- Students will be acquired the techniques to minimize the delays for better performance of a system on chip.
- Students will be acquired with the analytical skill to decide what type of processor is required to design anSoC for the undersigned application.
- Students will be calibre to classify the types and applications of different memory devices.
- Students will be able to analyze different types of buses for respective applications.
- Students will be skilful to judge a configurable device based on the application requirement for a system on chip
- Students will have the technique to implement AES algorithm if required.

UNIT –I

Introduction to the System Approach: System Architecture, Components of the system, Hardware & Software, Processor Architectures, Memory and Addressing. System level interconnection, An approach for SOC Design, System Architecture and Complexity.

UNIT –II

Processors: Introduction , Processor Selection for SOC, Basic concepts in Processor Architecture, Basic concepts in Processor Micro Architecture, Basic elements in Instruction handling. Buffers: minimizing Pipeline Delays, Branches, More Robust Processors, Vector Processors and Vector Instructions extensions, VLIW Processors, Superscalar Processors

UNIT –III

Memory Design for SOC: Overview of SOC external memory, Internal Memory, Size, Scratchpads and Cache memory, Cache Organization, Cache data, Write Policies, Strategies for line replacement at miss time, Types of Cache, Split – I, and D – Caches, Multilevel Caches, Virtual to real translation , SOC Memory System, Models of Simple Processor – memory interaction.

UNIT -IV

Interconnect Customization and Configuration: Inter Connect Architectures, Bus: Basic Architectures, SOC Standard Buses, Analytic Bus Models, Using the Bus model, Effects of Bus transactions and contention time. SOC Customization: An overview, Customizing Instruction Processor, Reconfiguration Technologies, Mapping design onto Reconfigurable devices, Instance-Specific design, Customizable Soft Processor, Reconfiguration - overhead analysis and trade-off analysis on reconfigurable Parallelism.

UNIT –V

Application Studies / Case Studies: SOC Design approach, AES algorithms, Design and evaluation, Image compression – JPEG
compression.

TEXT BOOKS

1. Computer System Design System-on-Chip - Michael J. Flynn and Wayne Luk, Wiely India Pvt. Ltd.
2. ARM System on Chip Architecture – Steve Furber –2nd Ed., 2000, Addison Wesley Professional.

REFERENCE BOOKS

1. Design of System on a Chip: Devices and Components – Ricardo Reis, 1st Ed., 2004, Springer
2. Co-Verification of Hardware and Software for ARM System on Chip Design (Embedded Technology) – Jason Andrews – Newnes, BK and CDROM.
3. System on Chip Verification – Methodologies and Techniques –Prakash Rashinkar, Peter Paterson and Leena Singh L, 2001, Kluwer Academic Publishers.

GOKARAJU RANGARAJU

INSTITUTE OF ENGINEERING AND TECHNOLOGY

WIRELESS LANS AND PANS
(ELECTIVE-IV)

M.Tech (ES) I Year - II Semester

Course Code: GR17D5092 L/T/P/C :3/1/0/4

COURSE OBJECTIVES

- To describe the basic concepts and principles of Wireless Systems
- To study the protocols and standards and architecture of Wireless Networks
- To introduce the student to the major concepts involving Wireless LANs (WLANs)
- To introduce Personal Area Network (PANs) concepts
- To describe the important issues and concerns involved in the Wireless Networks
- To design mobile/wireless communication system.
- To develop students' writing and research skills.

COURSE OUTCOMES: After going through this course the student will be able to

- An ability to explain about Wireless Systems and Networks
- An understanding of the multiple division and modulation techniques used in LAN's and PAN's.
- An ability to adhere to the protocols and architecture while using Wireless Networks.
- An ability to decide which wireless standard is useful for different applications.
- An ability to work using WLANs and PANs.
- An ability to work on a design project related to wireless communication systems.
- An ability to read, understand and write scientific articles through term assignments.

UNIT –I

Wireless System & Random Access Protocols: Introduction, First and Second Generation Cellular Systems, Cellular Communications from 1G to 3G, Wireless 4G systems, The Wireless Spectrum; Random Access Methods: Pure ALOHA, Slotted ALOHA, Carrier Sense Multiple Access (CSMA), Carrier Sense Multiple Access with Collision Detection (CSMA/CD), Carrier Sense Multiple Access with Collision Avoidance (CSMA/CA).

UNIT –II

Wireless LANs: Introduction, importance of Wireless LANs, WLAN Topologies, Transmission Techniques: Wired Networks, Wireless Networks, comparison of wired and Wireless LANs; WLAN Technologies: Infrared technology, UHF narrowband technology, Spread Spectrum technology

UNIT –III:

The IEEE 802.11 Standard for Wireless LANs: Network Architecture, Physical layer, The Medium Access Control Layer; MAC Layer issues: Hidden Terminal Problem, Reliability, Collision avoidance, Congestion avoidance, Congestion control, Security, The IEEE 802.11e MAC protocol

UNIT –IV:

Wireless PANs: Introduction, importance of Wireless PANs, The Bluetooth technology: history and applications, technical overview, the Bluetooth specifications, piconet synchronization and Bluetooth clocks, Master-Slave Switch; Bluetooth security; Enhancements to Bluetooth: Bluetooth interference issues, Intra and Inter Piconet scheduling, Bridge selection, Traffic Engineering, QoS and Dynamics Slot Assignment, Scatternet formation.

UNIT –V

The IEEE 802.15 working Group for WPANs: The IEEE 802.15.3, The IEEE 802.15.4, ZigBee Technology, ZigBee components and network topologies, The IEEE 802.15.4 LR-WPAN Device architecture: Physical Layer, Data Link Layer, The Network Layer, Applications; IEEE 802.15.3a Ultra wideband.

TEXT BOOKS

1. Ad Hoc and Sensor Networks - Carlos de MoraisCordeiro and Dharma Prakash Agrawal, World Scientific, 2011.
2. Wireless Communications and Networking - Vijay K.Garg, Morgan Kaufmann Publishers, 2009.

REFERENCE BOOKS

1. Wireless Networks - KavehPahlaram, Prashant Krishnamurthy, PHI, 2002.
2. Wireless Communication- Marks Ciampor, JeorgeOlenewa, Cengage Learning, 2007.

GOKARAJU RANGARAJU

INSTITUTE OF ENGINEERING AND TECHNOLOGY

EMBEDDED SYSTEMS LAB

M.Tech (ES) I Year - II Semester

Course Code: GR17D5093 L/T/P/C : 0/0/4/2

COURSE OBJECTIVES

- To impart the knowledge of ARM processor architecture &its programming
- To extract the features of ARM processor and interfacing with different peripherals.
- To understand the concept of Assembly, Embedded C and ARM programming.
- To understand the use of RTOS with ARM processor on IDE.
- To Develop an application with ARM processor.

COURSE OUTCOMES: The student will be able to

- Acquire the knowledge of ARM Processor architecture & its programming.
- Work on ARM based Processors.
- Develop an application in Arduino IDE using ARM programming.
- Interface ARM Processor with different peripherals.
- Implement Ethernet based server using ARM.
- Develop various applications using SPI and I2C Protocols
- Define and Design a project on the exposure with ARM processor with RTOS.

Note

A. The following programs are to be implemented on ARM based Processors/Equivalent.
B. Minimum of 10 programs from Part –I and 6 programs from Part -II are to be conducted.

PART- I

The following Programs are to be implemented on ARM Processor

1. Simple Assembly Program for
   a. Addition | Subtraction | Multiplication | Division
   b. Operating Modes, System Calls and Interrupts
   c. Loops, Branches
2. Write an Assembly programs to configure and control General Purpose Input/Output (GPIO) port pins.
3. Write an Assembly programs to read digital values from external peripherals and execute them with the Target board.
4. Program for reading and writing of a file
5. Program to demonstrate Time delay program using built in Timer / Counter feature on IDE environment
6. Program to demonstrates a simple interrupt handler and setting up a timer

7. Program demonstrates setting up interrupt handlers. Press button to generate an interrupt and trace the program flow with debug terminal.
8. Program to Interface 8 Bit LED and Switch Interface
9. Program to implement Buzzer Interface on IDE environment
10. Program to Displaying a message in a 2 line x 16 Characters LCD display and verify the result in debug terminal.
11. Program to demonstrate I2C Interface on IDE environment
12. Program to demonstrate I2C Interface – Serial EEPROM
13. Demonstration of Serial communication. Transmission from Kit and reception from PC using Serial Port on IDE environment use debug terminal to trace the program.
14. Generation of PWM Signal
15. Program to demonstrate SD-MMC Card Interface.

PART- II

Write the following programs to understand the use of RTOS with ARM Processor on IDE Environment using ARM Tool chain and Library:

1. Create an application that creates two tasks that wait on a timer whilst the main task loops.
2. Write an application that creates a task which is scheduled when a button is pressed, which illustrates the use of an event set between an ISR and a task
3. Write an application that Demonstrates the interruptible ISRs(Requires timer to have higher priority than external interrupt button)
4. a).Write an application to Test message queues and memory blocks. b).Write an application to Test byte queues
5. Write an application that creates two tasks of the same priority and sets the time slice period to illustrate time slicing.

Interfacing Programs:

6. Write an application that creates a two task to Blinking two different LEDs at different Timings 7. Write an application that creates a two task displaying two different messages in LCD display in two lines.
8. Sending messages to mailbox by one task and reading the message from mailbox by another task.
9. Sending message to PC through serial port by three different tasks on priority Basis.
10. Basic Audio Processing on IDE environment.

OPEN ELECTIVE - II

GOKARAJU RANGARAJU

INSTITUTE OF ENGINEERING AND TECHNOLOGY

HUMAN COMPUTER INTERACTION
(Open Elective-II)

M.Tech (CSE) I Year - II Semester

Course Code: GR17D5184 L/T/P/C :3/1/0/4

COURSE OBJECTIVES: Students undergoing the course are expected to:

- Demonstrate an understanding of guidelines, principles, and theories influencing human computer interaction.
- Recognize how a computer system may be modified to include human diversity.
- Select an effective style for a specific application.
- Design mock ups and carry out user and expert evaluation of interfaces.
- Carry out the steps of experimental design, usability and experimental testing, and
- Evaluation of human computer interaction systems.
- Use the information sources available, and be aware of the methodologies and technologies supporting advances in HCI.

COURSE OUTCOMES: At the end of the course, the student will be able to:

- Describe what interaction design is and how it relates to human computer interaction and other fields.
- Describe the social mechanisms that are used by people to communicate and collaborate.
- Describe how technologies can be designed to change people's attitudes and behavior.
- Discuss how to plan and run a successful data gathering program.
- Discuss the difference between qualitative and quantitative data and analysis.
- Discuss the conceptual, practical, and ethical issues involved in evaluation.
- Describe how to perform two types of predictive techniques, GOMS and Fitts Law, and when to use them.

UNIT-I

Introduction: Importance of user Interface –definition, importance of good design. Benefits of good design. A brief history of Screen design. The graphical user interface –popularity of graphics, the concept of direct manipulation, graphical system, Characteristics, Web user – Interface popularity, characteristics-Principles of user interface.

UNIT-II

Design process: Human interaction with computers, importance of human characteristics human consideration, Human interaction speeds, Understanding business junctions.

UNIT-III

Screen Designing: Design goals –Screen planning and purpose, organizing screen elements, ordering of screen data and content –screen navigation and flow –Visually pleasing composition

–amount of information –focus and emphasis –presentation information simply and meaningfully –information retrieval on web –statistical graphics –Technological consideration in interface design.

UNIT-IV

Develop System Menus and Navigation Schemes-Select the proper kinds of Windows, -Select the proper Device based Controls, Choose the proper screen based controls.

UNIT-V

Mobile Ecosystem: Platforms, Application frameworks- Types of Mobile Applications: Widgets, Applications, Games- Mobile Information Architecture, Mobile 2.0, Mobile Design: Elements of Mobile Design, Tools.

Interaction Devices – Keyboard and Function Keys – Pointing Devices – Speech Recognition Digitization and Generation – Image and Video Display – Drivers.

TEXT BOOKS

1. The essential guide to user interface design, Wilbert O Galitz, Wiley Dreamtech.
2. Designing the user interface. 3rd Edition Ben Shneidermann, Pearson Education Asia
3. Brian Fling, “Mobile Design and Development”, First Edition, Reilly Media Inc., 2009

REFERENCE BOOKS

1. Human – Computer Interaction. Alan Dix, Janet Fincay, GreGoryd, Abowd, Russell Bealg, Pearson Education
2. Interaction Design Prece, Rogers, Sharps. Wiley Dreamtech.
3. User Interface Design, Soren Lauesen, Pearson Education.

GOKARAJU RANGARAJU

INSTITUTE OF ENGINEERING AND TECHNOLOGY

BIG DATA ANALYTICS
(Open Elective-II)

M.Tech (IT) I Year - II Semester

Course Code: GR17D5185 L/T/P/C :3/1/0/4

COURSE OBJECTIVES: The objective of the course is to provide the student:

- Understanding about big data for business intelligence
- Learning business case studies for big data analytics
- Learning about the cloud and big data
- Knowledge about risk management involved in big data
- Understandingnosql big data management
- Understanding about map reduce work flows.
- Capability to Perform map-reduce analytics using Hadoop and related tools

COURSE OUTCOMES: At the end of the course the student will be able to:

- Understand the importance of big data
- Understand challenges with big data
- Knowledge about the technological developments in big data environment
- Understanding about map reduce work flows
- Knowledge about nosql data environment.
- Analysis with Hadoop and related tools
- Capability of understanding the usage of big data in context to cloud and other technologies.

UNIT-I

INTRODUCTION TO BIG DATA What is big data, why big data, convergence of key trends , unstructured data ,industry examples of big data ,web analytics, big data and marketing, fraud and big data ,risk and big data ,credit risk management, big data in medicine, introduction to Hadoop open source technologies , cloud and big data

UNIT-II

UNDERSTANDING BIG DATA Types of digital data, characteristics of data, challenges with big data, definition of big data, big data analytics,data science, technologies in big data environments, CAP theorem.

UNIT-III

NOSQL DATA MANAGEMENT Introduction to NoSQL, aggregate data models, aggregates, key-value and document data Models, relationships, graph databases , schemaless databases ,materialized views, distribution models, sharding ,master-slave replication, peer-peer replication, sharing and replication

UNIT-IV

BASICS OF HADOOP Data format ,features of Hadoop, analyzing data with Hadoop , design of Hadoop distributed file system (HDFS) ,HDFS concepts, scaling out ,Hadoop streaming , Hadoop pipes, Hadoop related tools

UNIT- V

MAPREDUCE APPLICATIONS MapReduce workflows, unit tests with MRUnit , test data and local tests, anatomy of MapReduce job run ,classic Map-reduce, YARN ,failures in classic Map-reduce and YARN , job scheduling , shuffle and sort ,task execution, MapReduce types ,input formats, output formats

TEXT BOOKS

1. Seema Acharya,S.Chellappan,"Big Data and Analytics",Wiley,2014

REFERENCE BOOK

1. Michael Minelli, Michelle Chambers, and AmbigaDhiraj, "Big Data, Big Analytics: Emerging Business Intelligence and Analytic Trends for Today's Businesses", Wiley, 2013.
2. P. J. Sadalage and M. Fowler, "NoSQL Distilled: A Brief Guide to the Emerging World of Polyglot Persistence", Addison-Wesley Professional, 2012.
3. Tom White, "Hadoop: The Definitive Guide", Third Edition, O'Reilley, 2012.
4. Eric Sammer, "Hadoop Operations", O'Reilley, 2012.

GOKARAJU RANGARAJU

INSTITUTE OF ENGINEERING AND TECHNOLOGY

NEURAL AND FUZZY SYSTEMS
(Open Elective-II)

M.Tech (EEE) I Year - II Semester

Course Code: GR17D5186 L/T/P/C :3/1/0/4

PRE–REQUISITE: Control Systems, Power Systems, Mathematics, Physics.

COURSE OBJECTIVES: The objective of the course is to provide the student

- To introduce the students with the concepts of learning methods.
- To provide students with the artificial neural networks and their architecture.
- To familiarize the students with the various applications of artificial neural networks.
- To introduce the concepts of the fuzzy logic control and their real time applications.

COURSE OUTCOMES: At the end of the course the student will be able to

- Define the advances in neural networks
- Evaluate the design and control of fuzzy systems.
- Articulate the applications of fuzzy control block sets.
- Evaluate the design of various models in neural networks
- To analyze the techniques of various types of neural networks
- Evaluate the design and control of associative memories
- Techniques to Design fuzzy logic system

UNIT-I

Introduction to Neural Networks: Introduction, Humans and Computers, Organization of the Brain, Biological Neuron, Biological and Artificial Neuron Models, Hodgkin-Huxley Neuron Model, Integrate-and- Fire Neuron Model, Spiking Neuron Model, Characteristics of ANN, McCulloch-Pitts Model, Historical Developments, Potential Applications of ANN.

UNIT-II

Essentials of Artificial Neural Networks: Artificial Neuron Model, Operations of Artificial Neuron, Types of Neuron Activation Function, ANN Architectures, Classification Taxonomy of ANN – Connectivity, Neural Dynamics (Activation and Synaptic), Learning Strategy (Supervised, Unsupervised, Reinforcement), Learning Rules, Types of Application

Feed Forward Neural Networks

Introduction, Perceptron Models: Discrete, Continuous and Multi-Category, Training Algorithms: Discrete and Continuous Perceptron Networks, Perceptron Convergence theorem, Limitations of the Perceptron Model, Applications.

UNIT-III

Multilayer Feed forward Neural Networks

Credit Assignment Problem, Generalized Delta Rule, Derivation of Backpropagation (BP) Training, Summary of Backpropagation Algorithm, Kolmogorov Theorem, Learning Difficulties and Improvements.

Associative Memories

Paradigms of Associative Memory, Pattern Mathematics, Hebbian Learning, General Concepts of Associative Memory (Associative Matrix, Association Rules, Hamming Distance, The Linear Associator, Matrix Memories, Content Addressable Memory), Bidirectional Associative Memory (BAM) Architecture, BAM Training Algorithms: Storage and Recall Algorithm, BAM Energy Function, Proof of BAM Stability Theorem Architecture of Hopfield Network: Discrete and Continuous versions, Storage and Recall Algorithm, Stability Analysis, Capacity of the Hopfield Network.

UNIT-IV

Self-Organizing Maps (SOM) and Adaptive Resonance Theory (ART)

Introduction, Competitive Learning, Vector Quantization, Self-Organized Learning Networks, Kohonen Networks, Training Algorithms, Linear Vector Quantization, Stability-Plasticity Dilemma, Feed forward competition, Feedback Competition.

UNIT-V

Classical and Fuzzy Sets and Fuzzy Logic System Components

Introduction to classical sets - properties, Operations and relations; Fuzzy sets, Membership, Uncertainty, Operations, properties, fuzzy relations, cardinalities, membership functions. Fuzzification, Membership value assignment, development of rule base and decision making system, Defuzzification to crisp sets, Defuzzification methods.

Applications Neural network applications: Process identification, Function Approximation, control and Process Monitoring, fault diagnosis and load forecasting.

Fuzzy logic applications: Fuzzy logic control and Fuzzy classification.

TEACHING METHODOLOGIES

1. White board
2. PPTs
3. Seminars

TEXT BOOK

1. Neural Networks, Fuzzy logic, Genetic algorithms: synthesis and applications by Rajasekharan and G.A.VijayalakshmiPai – PHI Publication.

REFERENCE BOOKS

1. Introduction to Artificial Neural Systems - Jacek M. Zuarda, Jaico Publishing House, 1997.
2. Neural Engineering by C.Eliasmith and CH.Anderson, PHI
3. Neural Networks and Fuzzy Logic System by Bork Kosko, PHI Publications

GOKARAJU RANGARAJU

INSTITUTE OF ENGINEERING AND TECHNOLOGY

PROJECT MANAGEMENT

M.Tech(Civil) I Year - II Semester

Course Code: GR17D5187 L/T/P/C :3/1/0/4

COURSE OBJECTIVES: On completion of this Subject/Course, following objectives shall get accomplished

- To provide students about the basics of Management in general and Project Management in particular.
- To train the students about the Monitoring of Projects.
- To make understand the students about the Planning of projects.
- To make understand the students about the Scheduling of projects.
- To train the students about the drawing of CPM & PERT Networks.
- To train the students about teaching of Project Management to UG & PG students
- To motivate the students about the Research Development activities of Project Management which results in timely completion of projects without time and cost over runs.

Course outcomes: On completion of this Subject/Course the student shall be able to

- Perform the Project Management functions effectively.
- Plan the projects.
- Schedule the various activities of Projects.
- Monitor the actual progress with planned progress.
- Draw the CPM & PERT Networks/
- Handle Resources planning including levelling & smoothing.
- Interpret the Indian Contract Act and understand the litigations involved for better Contract Management.

UNIT- I

PROJECT PLANNING: Prime Objectives of Project Management, Main Functions of Project Management, Planning, Principles of Planning, Objectives of Planning, Steps involved in Planning, Stages of Planning, Advantages & limitations of Planning, Failures of Projects & Construction Projects.

UNIT-II

PROJECT SCHEDULING: Scheduling, Project/Construction Schedules, Steps involved in Scheduling, Methods of Scheduling, Bar Charts, Steps involved in Bar Charts, Limitations of Bar Charts, Milestone Charts and Limitations of Milestone Charts.

UNIT-III

PROJECT MONITORING: Network Techniques, Prime Objectives of Networks, Network Terminology, Types of Networks, CPM & PERT, Differences between CPM & PERT, Rules to draw the Network, Drawing of Networks, Advantages of Network , Critical Path, Float and its Types, Slack and Types of Slack.

UNIT-IV

PROJECT COST CONTROL: Direct Costs, Indirect Costs, Total Project Cost, Optimisation of Cost and Steps involved, Resources, Resources Smoothing and Resources Levelling, Crashing of Activities, Time and Cost Over runs of Project.

UNIT-V

PROJECT QUALITY & CONTRACTS:

Quality, Quality Control, Quality Assurance, Project Quality Plans in Construction Projects, Inspection & Test Plans, Method Statements, ISO Certification; Project Contracts, Contract Law, Types of Contracts and Indian Contract Act.

TEXT BOOKS

1. Project Planning and Control with PERT & CPM – BC Punmia, KK Khandielwala.
2. Project Scheduling & Monitoring in Practice – S Chowdhury

REFERENCE BOOKS

1. Project Management Handbook – Lock, Gower
2. Project Management – NJ Smith- Blackwell Publication.

GOKARAJU RANGARAJU

INSTITUTE OF ENGINEERING AND TECHNOLOGY

HARDWARE - SOFTWARE CO-DESIGN
(Open Elective-II)

M.Tech (ECE) I Year - II Semester

Course Code: GR17D5188 L/T/P/C :3/1/0/4

Course Objectives

- Describe an embedded system design flow from specification to physical realization
- Describe structural behavior of systems.
- Master complex systems.
- Devise new theories, techniques, and tools in design, implementation and testing.
- Master contemporary development techniques.

Course Outcomes: After going through this course the student will be able to

- Gain knowledge of contemporary issues and algorithms used.
- Know the interfacing components, different verification techniques and tools.
- Demonstrate practical skills in the construction of prototypes.
- Understand the use of modern hardware and software tools for building prototypes of embedded systems.
- Apply embedded software techniques to satisfy functional and response time requirements.
- Apply verification tools.
- Understand design representation for system level synthesis.

UNIT-I:

Co- Design Issues: Co- Design Models, Architectures, Languages, A Generic Co-design Methodology.

Co- Synthesis Algorithms:

Hardware software synthesis algorithms: hardware – software partitioning distributed system cosynthesis.

UNIT –II:

Prototyping and Emulation: Prototyping and emulation techniques, prototyping and emulation environments, future developments in emulation and prototyping architecture specialization techniques, system communication infrastructure

Target Architectures: Architecture Specialization techniques, System Communication infrastructure, Target Architecture and Application System classes, Architecture for control dominated systems (8051-Architectures for High performance control), Architecture for Data dominated systems (ADSP21060, TMS320C60), Mixed Systems.

UNIT-III

Compilation Techniques and Tools for Embedded Processor Architectures: Modern embedded architectures, embedded software development needs, compilation technologies, practical consideration in a compiler development environment.

UNIT-IV

Design Specification and Verification: Design, co-design, the co-design computational model, concurrency coordinating concurrent computations, interfacing components, design verification, implementation verification, verification tools, interface verification

UNIT-V

Languages for System – Level Specification and Design-I: System – level specification, design representation for system level synthesis, system level specification languages,

Languages for System – Level Specification and Design-II:

Heterogeneous specifications and multi language co-simulation, the cosyma system and lycos system.

TEXT BOOKS

1. Hardware / Software Co- Design Principles and Practice – Jorgen Staunstrup, Wayne Wolf –2009, Springer.
2. Hardware / Software Co- Design - Giovanni De Micheli, Mariagiovanna Sami, 2002, Kluwer Academic Publishers

REFERENCE BOOKS

1. A Practical Introduction to Hardware/Software Co-design -Patrick R. Schaumont - 2010 –Springer

GOKARAJU RANGARAJU

INSTITUTE OF ENGINEERING AND TECHNOLOGY

NON CONVENTIONALENERGYRESOURCES

(Open Elective-II)

M.Tech (ME) I Year - II Semester
Course Code: GR17D5189

Course Objectives: The Objective of this course is to provide the student to

- Interduce the need of the non-convectional energy sources.
- Impart the role of non-convectional energy for the environment.
- Identify the energy resources utilization systems.
- Recognise the source and potential of wind energy and understand the classifications of wind mills.
- Summarize the principles of bio-conversion, ocean energy and geo thermal energy.

Course Outcomes: At the end of the course the learners will be able to

- Choose the appropriate renewable energy as an alternate for conventional power in any application.
- Analyze the environmental and cost economics of using renewable energy sources compared to fossil fuels.
- Apply the principles of various energy systems in day to day life.
- Analyze the industrial needs and convert theoretical model to practical circuits with wide range of specifications.
- Evaluate the importance of the renewable resources of energy as the fossil fuels are depleting in the world very fast express about clean and green energy for next generation.
- Analyse large scale demand of heat energy for meeting day to day domestic, institutional and industrial requirements can be met by utilizing solar thermal systems, biogas, PV cells, wind energy, Geothermal, MHD etc.
- Design the various techniques and models fabricated in utilizing the above said sources of energy.

UNIT-I

Introduction: Various non-conven tionalenergy resources-Introduction, availability, classification, relative merits and demerits.
Solar Cells: Theory of solarcells. solarcell materials, solarcellarray, solar callower plant, limitations.

UNIT-II

Solar Thermal Energy: Solar radiation, floatplane collectors and their materials, applications and performance, focusing of collectors and their materials, applications and performance; solar thermal power plants, thermal energy storage for solar heating and cooling, limitations.

UNIT-III

Geothermal Energy: Resources of geothermal energy, thermodynamics of geo-thermal energy conversion-electricalconversion, non-electricalconversion,environmentalconsiderations.
Magneto-hydrodynamics (MHD):
Principle of working of MHD Power plant, performance and limitations

FuelCells:

Principle of working of various type souffle cell sand their working, performance and limitations.

UNIT-IV

Thermos and the rmionic Conversions:
Principle of working, performance and limitations.
Wind Energy: Wind power and it surcease, sites election, criterion, momentum theory, classification of rotors, concentrations and augments, wind characteristics. Performance and limitation sofenergy conversion systems.

UNIT-V

Bio-mass: Availability of bio-massand its conversion theory.
Ocean Thermal Energy Conversion (OTEC):
Availability, theory and working principle, per formance and limitations.
Wave and Tida lWave:
Principle of working, performance and limitations.Waste RecyclingPlants.

TEXT/REFERENCESBOOKS

1. John Twideu and TonyWeir, “Renewal Energy Resources” BSP Publications, 2006.
2. M.V.R.KoteswaraRao, “Energy Resources: Conventional&Non-Conventional “ BSPPublications,2006.
3. D.S.Chauhan, ”Non-conventional Energy Resources” New Age International.
4. C.S. Solanki, “Renewal Energy Technologies: A Practical Guidefor Beginners” PHILearning.