Name And Designation: . Dr.G. Mamatha (Mamatha Samson)

Professor

Email ID: mamata2001@gmail.com

Educational Details: B.E, MS, Ph.D

Professional Background: Teaching -23 years Research -6 Years

Administrative Experience: PG Coordinator 3 years, Incharge HOD, ISTE Secretary, Coordinator for Women Development Cell

Committee Work: R&D Coordinator, M.Tech NBA Coordinator, Project Review Committee member,NAAC Coordinator,

Courses Taught:

UG classes	VLSI Design, VLSI Systems Design, DDTV HDL,STLD, Control Systems,VHDL, Signals and Systems, Electronic Circuits, Linear Integrated Circuits, Digital Integrated Circuits, Basic Electronics, Microelectronics, Communication Systems, Analog Communication, Measurements and Instrumentation, Power Electronicsetc
PG classes	VLSI Technology , Design for Testability ,Digital SystemDesign,CMOS Digital Integrated Circuits,CMOS Mixed Signal Circuits, CMOS Analog Integrated Circuits

PUBLICATIONS:

International Journals

[1] **Kadala Divyavani, Mamatha Samson, K.Swaraja, PadmavatiKora,Meenakshi.K "Design of Approximate Polar Maximum-Likelihood Decoder" in 'International Journal of Engineering and Advanced Technology (IJEAT)', ISSN: 2249-8958 (Online), Volume-9,Issue-2, December 2019, Page No 5086-5092.**

[2] **C. Leelavanthi, K Padmavathi, K Swaraja, K. Meenakshi " IoT Based Smart Surveillance System for Healthcare Monitoring using Raspberry PI"International Journal of Innovative Technology and Exploring Engineering Volume-8,Issue-12, October 2019, Page No 627-629**

[3] **K. Swaraja, K. Meenakshi, PadmavathiKora, Mamatha Samson, G. Karuna, A. Ushasree, "A Secure Architecture of Design for Testability" International Journal of Recent Technology and Engineering (IJRTE) ISSN: 2277-3878, Volume-8 Issue-2, July 2019**

[4] **PrashanthPerumadia, MamathaSamason,Optimized LLR 2^KB SCL Decoder for Polar Codes International Journal of Advanced Research Trends in Engineering and Technology (IJARTET) Vol.4, Issue 7, July2017**

[5] **P.Venu , Dr.Mamatha Samson "Design and implementation of an AreaEfficient Split-Radix FFT Processors UsingRadix-2 Butterfly Units" International Journal of Advanced Research Trends in Engineering and Technology(IJARTET) Vol.4, Issue 7, July2017**

[6] **K. Supriya, Dr. G. Mamatha," Implementation of optimal Encoder Architecure for long Polar Codes", IOSR Journal of VLSI and Signal Processing, Vol 6, Issue 6, Nov – Dec 2016, PP 87-95 7.**

[7] **RamagoniSwapnika, Dr. G. Mamatha," Content Addressable Memory Architecture based on SparseClustered Networks", IOSR Journal of VLSI and Signal Processing, Vol 6, Issue 6, Nov – Dec 2016, PP21-28**

[8] **MamathaSamson,Madhulatha "Energy Efficiency Enhancement for 45nm 1Mb SRAM Array Structures"International Journal of Computer Applications VOL105 No 5,November 2014,pp16-20**

[9] **Keerthi .V, Mamatha Samson "Design of BISTwith Low Power Test Pattern Generator"IOSR Journal of VLSI and Signal ProcessingVolume 4, Issue 5, Ver. II (Sep-Oct. 2014), pp 30-39**

[10] **Mamatha Samson "Effect of Phase of Noise on 6T SRAM cell", IOSR Journal of VLSI and Signal ProcessingVolume 4, Issue 3, Ver. I (May-Jun. 2014), pp 30-38**

[11] **Mamatha Samson Stable and Low Power 6T SRAM International Journal of Computer Applications VOL 78 NO 2 September 2013 pp 6 -10**

[12] **MamathaSamson,"Static Performance Analysis of Low power SRAM" IJCSNS International Journal of Computer Science and Network Security, VOL.10 No.5, May 2010, pp 189-195**

International Conferences:

[13] **Srilekha Kothapalli Mamata Samson,Sankararao Majji; Santoshchandra Rao K "A Novel Approach for High Gain Instrumentation Amplifier in DELTA SIGMA ADC", Journal: Materials Today: Proceedings (Accepted) https doi.org/10.1016/j.matpr.2020.01.441**

[14] **Bharath Kumar T., Samson M. (2020) Efficient SBT Architecture for HEVC. In: Kumar A., Paprzycki M., Gunjan V. (eds) ICDSMLA 2019. Lecture Notes in Electrical Engineering, vol 601. Springer, Singapore**

[15] **Anantoju L., Kora P., Samson M. (2020) Design of Delay and Energy Efficient Low Voltage Dual Tail Comparator by Using Sleep Transistor. In: Kumar A., Paprzycki M., Gunjan V. (eds) ICDSMLA 2019. Lecture Notes in Electrical Engineering, vol 601. Springer, Singapore**

[16] **Srilekha Kothapalli ; MamathaSamson Sankararao Majji ; Tulasi Radhika Patnala ; Santoshachandra Rao Karanam ; Chandra Sekhar Pasumarthi "Comparative Experimental Analysis of different Op-amps using 180nm CMOS Technology" Proceedings of 2020 International Conference on Emerging Trends in Information Technology and Engineering (ic-ETITE), Vellore India**

[17] **GaddeDondiSrinath, Mamatha Samson "Fault Tolerance in VLSI Circuit with Reducing Rollback Cost using FSM" Proceedings of 3rd IEEE Technically Sponsored International Conference on Computing Methodologies and Communication (ICCMC 2019) March 27-29, Erode, India. DOI:** 10.1109/ICCMC.2019.8819739

[18] **Mamatha Samson, L.Swetha "Remote Health Care System" Book Chapter inICICCT 2019 – System Reliability, Quality Control, Safety, Maintenance and Management : Applications to Electrical, Electronics and Computer Science and Engineering, Springer Singapore, pp.480-489 doi10.1007/978-981-13-8461-5, ISBN 978-981-13-8460-8**

[19] **HariKrishna Prasad Veerla,Mamatha Samson, "Optimized and Approximation Belief Propagation Decoder for Polar codes" International Conference on Trends in Information, Management, Enginering and Sciences, December 2018, pp. 87-91,Hyderabad,India**

[20] **Mamatha Samson, Satyam MandaValli "Adiabatic 5T SRAM" International Symposium on Electronic System Design (ISED) 2011 (IEEE Co sponsored) (19-21 December 2011, Kochi, India) (Presented the paper).**

[21] **Mamatha Samson, "Performance Analysis of Dual Vt Asymmetric SRAM -Effect of Process Induced VtVariations"International Conference on Advances in Computing, Control, and Telecommunication Technologies, ACT2009December 28-29, 2009, Trivandrum, Kerala, India.**

[22] **Mamatha Samson, M.B Srinivas "AnalyzingN-Curve Metrics for Sub-Threshold 65nm CMOS SRAM" proceedings of 8th IEEE Conference on Nanotechnology,2008.(Nano'08)pp 25-28,(2008)18-21 August ,Arlinton, Texas, U.S.A**

[23] **Mamatha Samson, M.B Srinivas "Read Stability and Write Ability Analysis of Dual –Vt Configurations of a single Cell of an SRAM Array-Effect of Process-Induced Intra-Die VtVariations"proceedings of 2NDIEEE International Nanoelectronics Conference(INEC008)pp 1015-1019,(2008)24-27 March, Shanghai, China**
(Presented the paper)

R & D Projects

Principle Investigator for WOS –A project sponsored by DST, Govt. of India on " Study and design of low power and high efficiency SRAM for memories" under the guidance of Dr. M. Satyam (Completed).

Review Work:

1. **The IEEE International Symposium on Circuits and Systems (ISCAS 2011)**
2. **IEEE Computer Society Annual Symposium on VLSI (ISVLSI 2013)**
3. **International Conference on Information Technology (ICIT 2014)**

4. Reviewer for Journals and Books:

International Journal of Electronics (Francis and Taylor)(Since 2009)

PROFESSIONAL WORK:

Talks/Paper Presentations:

1. **Speaker at Training Program by APHRDI, Govt. of Andhra Pradesh 2017**
2. **Speaker at Police Training, Govt. of Telangana, 2017-2018,2020**
3. **Speaker at Faculty Induction Program at GRIET 2017**

Seminars and Symposiums:

1. **Presented Paper at** of **2ND IEEE International Nanoelectronics Conference(INEC008)pp 1015-1019,(2008)24-27 March, Shanghai, China Presented Paper at International Symposium on**
2. **Presented Paper at Electronic System Design (ISED) 2011 (IEEE Co sponsored) (19-21 December 2011, Kochi, India**
3. **Attended International Conference on VLSI design and Embedded Systems (IEEE Co sponsored) India in 2007,2009,2010**

Memberships: ISTE, IEI, IEEE

External Examiner: Conducted Exams for M.Tech labs, M.Tech Project , B.Tech Project Exams and Paper Setting for prominent colleges of JNTUH and OU

AWARDS AND ACHIEVEMENTS: National Merit Scholarship -1986

CERTIFICATIONS: Associate Developer from National Instruments

Appreciations for NBA Coordination, Police Training, AAC Project Guidance, Moodle Course Development for VLSI Design