FACULTY PROFILE

Name : M.Kiran

Date of Birth : 20-11-1976

Highest Qualifications: M.Tech, (Ph.D)

Designation : Associate Professor

Qualification Details (From Highest Qualification)

S.No	Degree	University/ Institution/ Board	Year of passing	Class	Specialization
1	Ph.D	J.N.T.U.A., Anantapur		Continuing	Wireless Communications
2	M.Tech	J.N.T.U., Kakinada	March, 2007	First Class	Computers& Communications
3	B.Tech	VRSEC,Vijayawada, Acharya Nagarjuna University, Guntur.	April, 2001	First Class	Electronics& Communication Engineering
4	D.E.C.E.	Andhra Polytechnic, Kakinada. S.B.T.E.T.,Hyderabd	Sept, 1995	First Class	Electronics& Communication Engineering
5	S.S.C.	S.B.S.S.S.High School, Repalle.Board of Secondary Education, Hyderabad	March, 1992	First Class	

Experience:

Teaching:18 years.

Worked as Asst.Prof. in swarnandhra college of Engg.& Technology during sept,2001 to sept 2004. Worked as Asst.Prof in GRIET during Nov,2005 to June 2007. Worked as Sr.Asst.prof. in GRIET during June 2007 to Dec,2008. **Working as Associate Professor Jan 2008 to till date.**

Departmental activity	Modernization of labs &Workshops/Seminars/FDP Co-Ordinator Class Coordinator, Alumni coordinator, JNTU inspection Co-Ordinator
Institutional activity	TEQIP-II Nodal Officer (Academics)- March-2015-June-2017 QEEE CO-ORDINATOR- June- 2015-December-2015 ACE Valuation (Exam branch)- November-2014-November-2017

Publications/Conferences

[1] Nandam, K. S., Jamal, K., Budati, A. K., Mannem, K., & Kumar, M. O. (2020, June). Design of Multiplier with Dual Mode Based Approximate Full Adder. In *2020 5th International Conference on Communication and Electronics Systems (ICCES)* (pp. 40-46). IEEE.

[2] Jamal, K., Kiran Mannem, Manchalla OVP Kumar, and B. Veera Reddy. "FPGA Implementation of SIC Pair Generator." In *2020 5th International Conference on Communication and Electronics Systems (ICCES)*, pp. 62-67. IEEE, 2020.

[3] Pavan Kumar, M. O. V., and M. Kiran. "Design of optimal fast adder."*Advanced Computing and Communication Systems (ICACCS),* 2013 International Conference on. IEEE, 2013.

[4]

Publications/Conferences

[5] An Efficient VLSI Design of AES Cryptography in Memory Implementation Bijjam.Swathi, Manchalla.O.V.P.Kumar, G.Marlin Sheeba, M.Kiran, Y.Sudarsana Reddy

[6] Implementation of WFTA Structure in FFT processor based on memory E.Pravallika1, M.Kiran2, K.Jamal3, Manchalla.O.V.P.Kumar4
IJRECE(International Journal of Research in Electronics and Computer Engineering) vol. 6 issue 4 (october- december 2018)ISSN: 2393-9028 (print) | ISSN: 2348-2281 (online)

[7] Pari A.Labhe, K.Jamal, M.Kiran, "VLSI Design of a Novel BOSR Architecture for High Speed Applications" International Journal of Management, Technology And Engineering-ISSN NO : 2249-7455 Volume 8, Issue IX, SEPTEMBER/2018,Page No:115

[8] "Reconfigurable Multi-ASIP Architecture for Turbo Decoding" in IJARTET(International Journal of Advanced Research Trends in Engineering and Technology), Volume 4, Special Issue 9,April 2017. SRI, KOTTE USHA, and M. KIRAN. "Reconfigurable Multi-ASIP Architecture for Turbo Decoding."

[9] R.Sirisha , K.Jamal , M.Kiran "Programmable Pseudorandom Test Pattern Generator For BIST Implementation" IOSR Journal of VLSI and Signal Processing (IOSR-JVSP) Volume 6, Issue 6, Ver. III (Nov. - Dec. 2016), PP 58-63.

[10] CH. Yagnasri, M. Kiran, K. Jamal "Implementation of FM0 and Manchester Encoder for Efficient Hardware Utilization" IOSR Journal of VLSI and Signal Processing (IOSR-JVSP) Volume 6, Issue 6, Ver. III (Nov. - Dec. 2016), PP 12-20.

[11] M. Naveen Kumar, M.Kiran "Design and Implementation of DDR3 Controller with AXI Compliancy" *International Journal of Advanced Research in Computer and Communication EngineeringVol. 4, Issue 8, August 2015*

[12] L.Sujitha, M.Kiran "LUT Design Using OMS Technique for Memory Based Realization of FIR Filter" International Journal of Emerging Engineering Research and Technology Volume. 2, Issue 6, September 2014, PP 72-77

[13] B. Jayasri. M. Kiran "RISC Based Pipeline Architecture for Low Cost & Low Power Consumption of AES-GCM" International Journal of Engineering Associates (2320 – 0804) / # 103 / Volume 2 Issue 6-2013

Workshops Attended:

1. Faculty Development Program on Recent trends in Computer Architecture, VLSI and Embedded Systems RCAVES-2020 (08 -13 June 2020) organized by GRIET-ECE.
2. Participated FDP on PHP & MYSQL organized by JNTU jagityal from 18th May to 23rd May 2020.
3. Participated in the Webinar on the theme "Essence of Bhagavad Gita for Educators" by Swami Bodhamayananda, Director, VIHE, RKMath Hyderabad on 15 May 2020
4. Attended for attending the 2020 IEEE International Communications Quality and Reliability Workshop virtually held in online fashion on May 14, 2020
5. Participated on FDP online training on LaTex organized by IIT Bombay from 27th April to 2nd May 2020
6. Participated LTE Performance and Optimization Framework on 12th Feb 2020
7. Participated MU MIMO Massive MIMO and OFDM Technologies for 5G Networks from 27/3/2019 to 30/3/2019
8. Participated IEEE ComSoc Training "Fundamentals of 5G Small Cell Deployments" on 11th July 2018.
9. Participated FDP 201Xx Pedgogy for online and Blended Teaching-Learning process from 3rd May 2018 to 30th May 2018
10. Participated FDP 101x Foundation Program in ICT for Education [Part I] from 8rd March 2018 to 12th April 2018
11. Participated A Three day Workshop on ""Simulation and Emulation of Self Organized Networks (SEASON -2017)" from 14th October to 16th October 2017 at Kongu Engineering College, perundurai, Tamilnadu.
12. Participated FDP on " RF Antenna Design and Evaluation" from 15th May to 20th May 2017 at Vardhaman College of Engg., Hyderabad.
13. Participated GIAN course on "Spectrum Sharing in Next Generation Wireless Networks: Principles, Analysis & Case Studies" form 5-9 Sep-2016 at IIT Hyderabad.
14. Attended Ph.D Course work from 13th June 2016 to 25th June 2016
15. A two day workshop on "Advancements in Mobile Communications" at ANU Guntur during 24th-25thfeb 2016
16. Management Capacity Enhancement Programme ON October 27 - November 02, 2014 Under IIM Indore.
17. A two day workshop on "Aakash tablet for Engineering Education" under IITM during 10th-11th Nov.2012.

18. One week workshop on Staff Development Program on Embedded Systems Design from 2nd -7th Feb.2012
19. Trends in Researching Development an Academic perspective on 21st Aug, 2009 at JNTUH.

Workshops Organized:

1. Organized one week FDP on Arificial Intelligence and Machine Learning from 29th April 19 to 4th May 2019.
2. Orgnized Workshop on Smart Homes Measurements Grids using IoT,from10th to 12th October,2017,held at GRIET,Hyderabad.
3. Organized Workshop on Embedded Systems Using TivaC, Orbit Booster Pack & Energia, 15-16 Dec-2016. held at GRIET, Hyderabad.
4. Organized Workshop on Embedded Systems Using TivaC, Orbit Booster Pack & Energia, 6-7,Dec-2016. held at GRIET, Hyderabad
5. Organized Hands on IOT workshop on " sensor to cloud" Oct 19-21, 2016
6. Organized Three day FDP on VLSIDSP during 28th -30th Jan 2016.
7. Three day FDP on Estimation Theory on CRN from 15 Oct to 17 Oct 2015.
8. One week workshop on Digital Design using Cadence Tools From 12th to 16th March, 2012
9. One week workshop on Digital Design through FPGA From 5th to 9th March, 2012
10. One week workshop on Analog & Digital Signal Design using Cadence Tools 27th Oct. 2011 to 01 Nov.2011
11. Organizing member for ICMID-2010 during 17th-19th December2010
12. A one week workshop on "Digital Design through FPGA" From 5th To 10 Apr. 2010 at GRIET
13. A one week workshop on "Digital Design through FPGA" From 8th To 13 Feb. 2010 at GRIET
14. A National level Staff Development Program sponsored by AICTE titled " Embedded System Design" during 15th-27th June2009 at GRIET Hyderabad.

PG Projects:

1. Implementation of WFTA Structure in FFT processor based on memory-A.Y.2018-19
2. A Memory based FFT processor Design with generalized efficient conflict-free address schemes-A.Y.2017-2018
3. Reconfigurable Multi-ASIP Architecture For Turbo Decoding-A.Y.2016-17
4. Implementation of FM0 and Manchester Encoder for Efficient Hardware Utilization-A.Y.2015-16
5. Design and Implementation of DDR3 Controller with AXI Compliancy- A.Y.2014-15
6. LUT Design Using OMS Technique for Memory Based Realization of FIR Filter-A.Y.2013-14
7. Crypto Instructions-Aware RISC Processor-A.Y.2012-13
8.

UG Projects:

1. A comprehensive study on hand off management in LTE and LTE Advanced using NS2 A.Y 2019-2020
2. Automatic Energy Management in 4G/5G LTE Networks using Machine Learning Algorithms A.Y- 2018-19
3. Dedicated Core Network Selection based on UE usage type-A.Y.-2017-18
4. Latency based Routing-SDN-A.Y.-2015-16
5. Implementation of convolution Encoder and Viterbi Decoder- A.Y.-2013-2014
6. Design of RISC Processor(64-bit) IP Core-A.Y.-2012-2013
7. Flip-chip Physical Verification Using Calibre- A.Y.-2012-2013
8. Implementation of carrier recovery with digital modulation schemes- A.Y.-2012-2013
9. Wireless Data Encryption and Decryption for Secured Communication - A.Y.-2012-2013
10. FPGA Implementation of RS232 to Universal serial bus converter- A.Y.2011-2012
11. Implementation of Exchange Server (Electronic Messaging system) with Mail Security in a Corporate Network- A.Y.2011-2012
12. 32-bit 33MHz PCI Target Interface-A.Y.2010-2011
13. Implementation of spanning tree protocol- A.Y.2010-2011
14.

Area of Interest: Wireless Communications,Networking

Contact:

Phone Number: 9440457027
Email ID:**kiranmannem14@gmail.com, kiran_m_20@rediffmail.com**

(M.Kiran)