Faculty Profile

Name And Designation: Dr. D.Jayanthi

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Educational Details:

Si No	Degree	College	University / Country	Year	Specialization
1	Bachelor of Engineering (B.E.)	Periyar Maniammai College of Engineering and Technologyi	Bharathidasan Uinversity, India	1993	Electronics and Communication Engineering**(E.C.E)**
2	Master of Technology(M. Tech.)	SASTRA	SASTRA Uinversity, India	2002	VLSI Design
3	Ph.D.	----	Anna University, India	2013	VLSI Design

Professional Background:

S.no	Designation	Department	Institute /Organization	Period
1	Professor	Electronics and Communication Engineering	Gokaraju Rangaraju Institute of Engineering and Technology, Hyderabad.	12/12/2016 to till date…
2	Associate Professor	Electronics and Communication Engineering	Sona College of Technology, Salem Tamil Nadu	16/08/2005 to 11/12/2016
3	Assistant Professor	Electronics and Communication Engineering	KSR College of Technology,TamilNadu	2/12/2002 to 05/08/2005
4	Lecturer	Electronics and Communication Engineering	MAhendra Enigneering College,TamilNadu	16/06/1997 to 01/12/2002

Courses Taught:

- **UG:** VLSI Design Techniques, Digital Electronics, Communication System, Network Theory, Electronic Devices, Computer Organization
- **PG:** CMOS VLSI Design, CAD For VLSI, ASIC Design, System-on- Chip, Digital System Design

PUBLICATIONS:

1. Jayanthi. D.and Rajaram.M.,"Design and Analysis of Asynchronous Pipeline Controller"- "European Journal of Scientific Research"ISSN 1450-216X Vol.72 No.1 (2012), pp. 84-91.

2. Jayanthi. D.and Rajaram.M.,"A Quasi Delay Insensitive ReducedStack Pre-Charged Half Buffer based High Speed Adder using pipeline templates for Asynchronous Circuits" Journal of Computer Science 8 (7): 1114-1122, 2012, ISSN 1549-3636,pp. 1114-11122.

3. Jayanthi. D.and Rajaram.M.,"The Design of High Performance Asynchronous Pipelines with Quasi Delay Insensitive"International Journal of Computer Applications ,Volume 52– No.16, pp35-41., August 2012.

4. Jayanthi. D.and Rajaram.M.,"High Performance Asynchronous pipelined QDI templates for DCT Matrix-vector Multiplication"International Journal of Computer Applications (0975 – 8887) Volume 55– No.17, pp44-51., October 2012.

5. D.Jayanthi "Logical Effort for SCV-Based Ripple Carry Adder" International Journal of Applied Engineering Research, ISSN 0973-4562 Vol. 10 No.55 PP 81-86, 2015.

6. Arun vignesh N,Jayanthi.D "Design of FIR filter Architecture using Manifold Steady Method"International Journal of Applied Engineering Research,ISSN 2455-4847 Vol.02-Issue 08,PP20-26,Aug 2017.

7. D.Jayanthi,A.Bhavani Shankar,S.Raghavan and G Rajasekar,"High Speed Multioutput Circuits Using Adiabatic Logic" 978-1-4673-6725-7/16/$31.00 ©2016 IEEE

8. Bandike. Dinesh Kumar, D. Jayanthi, N. Arun Vignesh, K. Jamal "Area Efficient Design of BIST Technique in UART using Circuit under Test (CUT)" International Journal of Recent Technology and Engineering (IJRTE) ISSN: 2277-3878, Volume-8 Issue-5, January 2020

9. Tulasi Radhika Patnala,D.Jayanthi,Sankararao Majji,"A Modernistic way for KEY Generation for Highly Secure Data Transfer in ASIC Design Flow" 2020 6th International Conference on Advanced Computing & Communication Systems; 978-1-7281-5197-7/20/$31.00 ©2020 IEEE

10. Tulasi Radhika Patnala,D.Jayanthi ,"Maximal length test pattern generation for the cryptography Application",Proceedings-Materials Today(Article in Press)

PROFESSIONAL WORK:

1. **Published patent in the year of 2018 titled as " MRI TUMOR IMAGE RETRIEVAL FOR SUPPORTING COMPUTER AIDED DIAGNOSIS"**
2. **Received fund of Rs 14.6 Lakhs from AICTE to create Skills and Personality Development Centre**

Memberships:

IEEE, Life member in ISTE

External Examiner :

M.Tech HDL Simulation Lab Examiner

AWARDS AND ACHIEVEMENTS:

Si. No	Name and Nature of the Award / Honor	Issued at Organization / Event	Year of Award
1	Best Project Award	AICTE	2007
2	Best Project Award and Fund Received	TamilNadu State council for Science and Technology,Chennai.	2010