ACADEMIC REGULATIONS

PROGRAM STRUCTURE

and

DETAILED SYLLABUS

Master of Technology

(VLSI)

(Two Year Regular Programme)

(Applicable for Batches admitted from 2018

Gokaraju Rangaraju Institute of Engineering and

Technology (Autonomous)

Bachupally, Kukatpally, Hyderabad- 500 090

Academic Regulations

GOKARAJU RANGARAJU
INSTITUTE OF ENGINEERING AND TECHNOLOGY, HYDERABAD
For all Post Graduate Programmes (M.Tech)
GR18 REGULATIONS

Gokaraju Rangaraju Institute of Engineering & Technology - 2018 Regulations (GR 18 Regulations) are given hereunder. These regulations govern all the Post Graduate programmes offered by various departments of Engineering with effect from the students admitted to the programmes in 2018-19 academic year.

1. **Programme Offered:** The Post Graduate programme offered by the department is M.Tech, a two-year regular programme in that discipline.
2. **Medium of Instruction:** The medium of instruction (including examinations and reports) is English.
3. **Admissions:** Admission into the M.Tech Programme in any discipline shall be made subject to the eligibility and qualifications prescribed by the University from time to time. Admissions shall be made either on the basis of the merit rank obtained by the student in PGCET conducted by the APSCHE for M. Tech Programmes or on the basis of any other order of merit approved by the University, subject to reservations as prescribed by the Government from time to time.
4. **Programme Pattern:**
    - **a) A student is introduced to "Choice Based Credit System (CBCS)" for which he/she has to register for the courses at the beginning of each semester as per the procedure.**
    - b) Each Academic year of study is divided into two semesters.
    - c) Minimum number of instruction days in each semester is 90.
    - d) The total credits for the Programme is 68.
    - **e) Grade points, based on percentage of marks awarded for each course will form the basis for calculation of SGPA (Semester Grade Point Average) and CGPA (Cumulative Grade Point Average).**
    - **f) A student has a choice of registering for credits from the courses offered in the programme.**
    - **g) All the registered credits will be considered for the calculation of final CGPA.**
5. **Award of M.Tech Degree:** A student will be declared eligible for the award of the M. Tech Degree if he/she fulfills the following academic requirements:
    - a) A student shall be declared eligible for the award of M.Tech degree, if he/she pursues the course of study and completes it successfully in not less than two academic years and not more than four academic years.
    - b) A Student, who fails to fulfill all the academic requirements for the award of the degree within four academic years from the date of admission, shall forfeit his/her seat in M.Tech course.
    - c) The Degree of M.Tech shall be conferred by Jawaharlal Nehru Technological University Hyderabad (JNTUH), Hyderabad, on the students who are admitted to the programme and fulfill all the requirements for the award of the degree.

6. Attendance Requirements

a) A student shall be eligible to appear for the semester end examinations if he/she puts in a minimum of 75% of attendance in aggregate in all the courses concerned in the semester.

b) Condonation of shortage of attendance in aggregate up to 10% (65% and above and below 75%) in a semester may be granted. A committee headed by Dean (Academic Affairs) shall be the deciding authority for granting the condonation.

c) Students who have been granted condonation shall pay a fee as decided by the Academic Council.

d) Students whose shortage of attendance is not condoned in any semester are detained and are not eligible to take their end examinations of that semester. They may seek re-registration for that semester when offered next with the academic regulations of the batch into which he/she gets re-registered.

7. Paper Setting, Evaluation of Answer Scripts, Marks and Assessment

a) Paper setting and Evaluation of the Answer Scripts shall be done as per the procedures laid down by the Academic Council of the College from time to time.

b) The following is the division of marks between internal and external evaluations.

Particulars	Internal Evaluation	External Evaluation	Total
Theory	30	70	100
Practical	30	70	100
Mini Project	30	70	100
Dissertation	30	70	100

c) The marks for internal evaluation per semester per theory course are divided as follows:

i.	**Mid Examinations:**	**20 Marks**
ii.	**Tutorials/Assignment:**	**5 Marks**
iii.	**Continuous Assessment:**	**5 Marks**
	Total:	**30 Marks**

d) **Mid Examination:** There shall be two mid examinations during a semester. The first mid examination shall be conducted from the first 50 per cent of the syllabus and the second mid examination shall be conducted from the remaining 50 per cent of the syllabus. The mid examinations shall be evaluated for **20 marks** and average of the marks scored in the two mid examinations shall be taken as the marks scored by each student in the mid examination for that semester.

e) **Assignment:** Assignments are to be given to the students and marks not exceeding 5 (5%) per semester per paper are to be awarded by the teacher concerned.

f. **For Internal Evaluation in Practical/Lab Subjects:** The marks for internal evaluation are 30. Internal Evaluation is done by the teacher concerned with the help of the other staff members nominated by Head of the Department. Marks Distribution is as follows:

i.	Internal Exam:	10 Marks
ii.	Record:	05 Marks
iii.	Continuous Assessment:	15 Marks
	Total:	30 Marks

g. For External Evaluation in Practical/Lab Subjects: The semester end examination shall be conducted by an external examiner and a staff member of the department nominated by Head of the Department.

h. For approval and evaluating mini-project, Dissertation-I and Dissertation-II, a project Review Committee (PRC) will be constituted by the Head of the Department. The composition of PRC is as follows

i) Head of the Department

ii) One senior faculty relevant to the specialization

iii) Coordinator of the specialization.

i. Mini Project: The Mini Project is to be taken up with relevance to Industry and is evaluated for 100 marks .Out of 100 marks, 30 marks are for internal evaluation and 70 marks are for external evaluation.

Internal Evaluation:

For internal evaluation,10 Marks are given by PRC based on project reviews and 5 marks for the quality of report and abstract submitted. The supervisor continuously assesses the student performance for 15 marks. Tentative presentation dates and marks distribution of the mini-project

S.No	Date	Review	Marks
Internal Marks (30)			
1	First week of the semester	Abstract submission*	5
2	Mid of the semester	Second review	10
3	Last week of the semester	Last review	15

*Following are the guidelines for the abstract submission

The faculty are requested to check the document submitted in the first review and should contain following

1. Title of the project and Literature review
2. Schematic/Block diagram which gives the board idea of the entire project (Mini project to major

project in 3rd and 4thsemesters)

3. Timeline or milestone of the project. It should clearly indicate deliverables/outcomes of the project.
4. Components required with approximate cost
5. References

External Evolution: (70 Marks)

The mini project report is presented before PRC along with the supervisor and the same is evaluated for 70 marks. At the end of the semester the mini-project report is evaluated by PRC.

Guidelines to award 70 marks:

S.No	Date	Review/ PRC report	Marks
External Evaluation Marks (70)			
1	Last week of the semester	FinalPresentation andreport Submission	10
2	Project report :Project report should be written as per IEEE guidelines.	Verified by PRC	20
3	Project Deliverables • Hardwareprototype • Simulation in any authorizedsoftware • Submission of research articles in anyScopus indexedconference /Journal	Verified by PRC	30
4	Results and Discussion	Verified by PRC	10

ii. Dissertation(Phase-I&Phase-II):

Internships/Seminars/Dissertation Phase-I:

The Dissertation Phase-I, the department help the students to do the projects supported by the industry and is evaluated for 100marks.Out of 100marks, 30marks are for internal evaluation and 70 marks are for external evaluation.

Internal Evaluation: For internal evaluation, 10Marks are given by the PRC based on project reviews and 5 marks for the quality of report and abstract submitted. The supervisor continuously assesses the student performance for 15marks.Tentative presentation dates and marks distribution of the Dissertation Phase-I.

S.No	Date	Review	Marks
Internal Marks (30)			
1	lst week of the semester	Abstract submission*	5
2	Mid of the semester	Second review	10
3	Last week of the semester	Last review	15

*Following are the guidelines for the abstract submission

The faculty are requested to check the document submitted in the first review and should contain following

1. Title of the project and the literature review
2. Schematic/Block diagram which gives the board idea of the entire project
3. Timeline or milestone of the project. It should clearly indicate deliverables/outcomes of the project.
4. Components required with approximate cost
5. Possibility to develop Product

External Evolution: (70 Marks)

The mini project report is presented before PRC along with the supervisor and the same is evaluated for 70 marks. At the end of the semester the mini project report is evaluated by PRC.

Guidelines to award 70 marks:

S.No	Date	Review/ PRC report	Marks
External Evaluation Marks (70)			
1	Last week of the semester	Final Presentation and report Submission	10
2	Project report submission- Project report should be written as per IEEE guidelines.	Verified by PRC	20

3	Project Deliverables • Hardwareprototype • Simulations in any authorizedsoftware • Submission of research articles in any Scopus indexed conference /Journal • Productdevelopment • IndustrySupport	Verified by PRC	30
4	Results and Discussion	Verified by PRC	10

iii. Dissertation Phase-II :Dissertation

Phase II:

The Dissertation Phase -II, the department help the students to do the project at industry and is evaluated for 100 marks. Out of 100 marks, 30 marks are for internal evaluation and 70 marks are for external evaluation. It is expected that along with the project he will be placed in the company.

Internal Evaluation: For internal evaluation,10 Marks are given by the PRC based on project reviews and 5 marks for the quality of report and abstract submitted. The supervisor continuouslyassessesthestudentperformancefor15marks.Tentativepresentationdatesand marks distribution of the mini-project

S.No	Date	Review	Marks
Internal Marks (30)			
1	lst week of the semester	Abstract submission*	5
2	Mid of the semester	Second review	10
3	Last week of the semester	Last review	15

*Following are the guidelines for the abstract submission

The faculty are requested to check the document submitted in the first review and should contain following

1. Title of the project and the literature review
2. Schematic/Block diagram which gives the board idea of the entire project
3. Timelineormilestoneoftheproject.Itshouldclearlyindicatedeliverables/outcomes of the project.
4. Components required with approximate cost
5. Possibility to develop Product and IPR

External Evolution: (70 Marks)

The project report is presented before PRC along with the supervisor and the same is evaluated for 70 marks. At the end of the semester the project report is evaluated by PRC.

Guidelines to award 70 marks:

S.No	Date	Review/ PRC report	Marks
External Evaluation Marks (70)			
1	Last week of the semester	Final Presentation and report Submission	10
2	Project report submission- Project report should be written as per IEEE guidelines.	Verified by PRC and External Examiner	20
3	Project Deliverables • Hardware prototype • Simulations in any authorized software • Submission of research articles in any Scopus indexed conference /Journal • Product development • Industry Support	Verified by PRC and External Examiner	30
4	Results and Discussion	Verified by PRC and External Examiner	10

Rules and regulations related to Internships/Seminars/Dissertation Phase I and II:

The student must work under the guidance of both internal guide (one faculty member of the department) and external guide (from Industry not below the rank of an officer).Internal guide is allotted by the Head of the Department or Program Coordinator, where as external guide is allotted by the industrial organization in which the project is under taken.

- After approval from the PRC, the final thesis is to be submitted along with ANTI- PLAGIARISM report from the approved agency with a similarity index not more than 24%.
- Two hardcopies and one soft copy of the project work (dissertation) certified by the research supervisors shall be submitted to the College/Institute.

- The thesis shall be adjudicated by one external examiner selected by the Institute out of 5-member panel, submitted by the department.
- In both internal and external evaluations, the student shall score at least 40% marks and anaggregate of 50% marks to pass in the project work. If the project report is satisfactory, Viva-voce examination shall be conducted by a Board consisting of the Supervisor, Head and the External Examiner who adjudicated the project work. The Board shall jointly evaluate the student's performance in the project work.
- In case the student doesn't pass through the project work, he/she must reappear for the viva-voce examination, as per the recommendations of the Board. If he fails succeed at the second Viva-voce examination also, he will not be eligible for the award of the degree, unless she/he is asked to revise and resubmit the Project by the Board. Head of the Department and program coordinator shall coordinate and make arrangements for the conduct o fviva-voce examination. When one does get the required minimum marks both in internal and external evaluations the candidate has to revise and resubmit the dissertation in the time frame prescribed by the PRC. If the report of the examiner is unfavorable again, the project shall be summarily rejected.
- If a student gets a chance to work in industry for one year (placement through internship) then he/she should take permission from Principal, Dean of examinations, Dean of Placements, Dean Academics, Department HOD and program coordinator. He/she should complete the credits in 3rd semester in consultation with course instructor and program coordinator.

8. **Recounting of Marks in the End Examination Answer Books:** A student can request for re-counting of his/her answer book on payment of a prescribed fee.

9. **Re-evaluation of the End Examination Answer Books:** A student can request for re-evaluation of his/her answer book on payment of a prescribed fee.

10. **Supplementary Examinations:** A student who has failed in an end semester examination can appear for a supplementary examination, as per the schedule announced by the College/Institute.

11. **Malpractices in Examinations:** Disciplinary action shall be taken in case of malpractices during Mid/ End-examinations as per the rules framed by the Academic Council.

12. **Academic Requirements:**

    a) A student shall be deemed to have secured the minimum academic requirement in a subject if he / she secures a minimum of 40% of marks in the Semester-end Examination and a minimum aggregate of 50% of the total marks in the Semester-end examination and Internal Evaluation taken together.

    b) A student shall be promoted to the next semester only when he/she satisfies the requirements of all the previous semesters.

c) In order to qualify for the award of M.Tech Degree, the student shall complete the academic requirements of passing in all the Courses as per the course structure including Seminars and Project if any.

d) In case a Student does not secure the minimum academic requirement in any course, he/she has to reappear for the Semester-end Examination in the course, or re-register for the same course when next offered or re-register for any other specified course, as may be required. However, one more additional chance may be provided for each student, for improving the internal marks provided the internal marks secured by a student are less than 50% and he/she failed finally in the course concerned. In the event of taking another chance for re-registration, the internal marks obtained in the previous attempt are nullified. In case of re-registration, the student has to pay the re-registration fee for each course, as specified by the College.

e) Grade Points: A 10- point grading system with corresponding letter grades and percentage of marks, as given below, is followed:

Letter Grade	Grade Points	Percentage of marks
O (Outstanding)	**10**	**Marks >= 90**
A+ (Excellent)	**9**	**Marks >= 80 and Marks < 90**
A (Very Good)	**8**	**Marks >= 70 and Marks < 80**
B+ (Good)	**7**	**Marks >= 60 and Marks < 70**
B (Above Average)	**6**	**Marks >= 50 and Marks < 60**
F (Fail)	**0**	**Marks < 50**
Ab (Absent)	**0**	

Earning of Credit:

A student shall be considered to have completed a course successfully and earned the credits if he/she secures an acceptable letter grade in the range O-C. Letter grade 'F' in any Course implies failure of the student in that course and no credits earned. Computation of SGPA and CGPA:

The UGC recommends the following procedure to compute the Semester Grade Point Average (SGPA) and Cumulative Grade Point Average (CGPA):

i) S_k the SGPA of k^{th} semester(1 to 4) is the ratio of sum of the product of the number of credits and grade points to the total credits of all courses registered by a student, i.e.,

$$\text{SGPA } (S_k) = \sum_{i=1}^{n} (C_i * G_i) / \sum_{i=1}^{n} C_i$$

Where C_i is the number of credits of the i^{th} course and G_i is the grade point scored by the student in the i^{th} course and n is the number of courses registered in that semester.

ii) The CGPA is calculated in the same manner taking into account all the courses m, registered by a student over all the semesters of a programme, i.e., upto and inclusive of S_k, where $k \geq 2$.

$$\text{CGPA} = \sum_{i=1}^{m} (C_i * G_i) / \sum_{i=1}^{m} C_i$$

iii) The SGPA and CGPA shall be rounded off to 2 decimal points.

13. **Award of Class:** After a student satisfies all the requirements prescribed for the completion of the Degree and becomes eligible for the award of M. Tech Degree by JNTUH, he/she shall be placed in one of the following four classes:

	Class Awarded	CGPA Secured
13.1	First Class With Distinction	CGPA ≥ 7.75
13.2	First Class	CGPA ≥ 6.75 and CGPA < 7.75
13.3	Second Class	CGPA ≥ 6.00 and CGPA < 6.75

14. **Withholding of Results:** If the student has not paid dues to the Institute/ University, or if any case of indiscipline is pending against him, the result of the student (for that Semester) may be withheld and he will not be allowed to go into the next Semester. The award or issue of the Degree may also be withheld in such cases.

15. **Transfer of students from the Constituent Colleges of JNTUH or from other Colleges/ Universities:** Transfer of students from the Constituent Colleges of JNTUH or from other Colleges/ Universities shall be considered only on case-to-case basis by the Academic Council of the Institute.

16. **Transitory Regulations:** Students who have discontinued or have been detained for want of attendance, or who have failed after having undergone the Degree Programme, may be considered eligible for readmission to the same or equivalent subjects as and when they are offered.

17. General Rules

a) The academic regulations should be read as a whole for the purpose of any interpretation.

b) In the case of any doubt or ambiguity in the interpretation of the above rules, the decision of the Academic Council is final.

c) In case of any error in the above rules and regulations, the decision of the Academic Council is final.

d) The college may change or amend the academic regulations or syllabi at any time and the changes or amendments made shall be applicable to all the students with effect from the dates notified by the college.

Gokaraju Rangaraju Institute of Engineering and Technology
Department of Electronics and communication Engineering
VLSI

I YEAR - I SEMESTER

Sl. No	Group	Subject Code	Subject	Credits			Credits	Int. Marks	Ext. Marks	Total Marks
				L	T	P				
1	Core I	GR18D5076	Digital System Design using HDL	3	-	-	3	30	70	100
2	Core II	GR18D5077	Digital CMOS IC Design	3	-	-	3	30	70	100
3	**PE I**	GR18D5078 GR18D5079 GR18D5080	1.Digital System Design 2.Device Modeling 3.Scripting Languages	3	-	-	3	30	70	100
4	**PE II**	GR18D5081 GR18D5082 GR18D5083	1.CPLD and FPGA Architecture 2.Micro Controllers for Embedded Systems 3.VLSI Technology and Design	3	-	-	3	30	70	100
5	Core	GR18D5084	HDL Simulation Lab	-	-	4	2	30	70	100
6	Core	GR18D5085	Digital CMOS IC Design Lab	-	-	4	2	30	70	100
7	Core	GR18D5012	Research Methodology and IPR	2	-	-	2	30	70	100
8	Audit		Audit course -1	2	-	-	0	30	70	100
		Total		**16**	**-**	**8**	**18**	**240**	**560**	**800**

I YEAR - IISEMESTER

Sl. No	Group	Subject code	Subject	Credits			Credits	Int. Marks	Ext. Marks	Total Marks
				L	T	P				
1	Core III	GR18D5086	Analog COMS IC Design	3	-	-	3	30	70	100
2	Core IV	GR18D5087	ASIC Design	3	-	-	3	30	70	100
3	**PE III**	GR18D5088 GR18D5089 GR18D5090	1.Optimizations Techniques in VLSI Design 2.System on Chip Architecture 3.Design for Testability	3	-	-	3	30	70	100
4	**PE IV**	GR18D5091 GR18D5092 GR18D5093	1.Digital Signal Processors and Architecture 2.Low Power VLSI Design 3.Hardware Software Co Design	3	-	-	3	30	70	100
5	Core	GR18D5094	Analog CMOS IC Design Lab	-	-	4	2	30	70	100
6	Core	GR18D5095	ASIC Design Lab	-	-	4	2	30	70	100
7	Audit		Audit course – 2	2	-	-	0	30	70	100
8	Core	GR18D5190	Mini-Project	2	-	-	2	30	70	100
		Total		**16**	**-**	**8**	**18**	**240**	**560**	**800**

II YEAR - ISEMESTER

Sl. No	Group	Subject code	Subject	Credits L	Credits T	Credits P	Credits	Int. Marks	Ext. Marks	Total Marks
1	**PE V**	GR18D5096 GR18D5097 GR18D5098	1. Advanced Computer Architecture 2. CAD for VLSI 3. CMOS Mixed Signal Circuit Design		-	-	3	30	70	100
2	**Open Elective**	GR18D5201 GR18D5202 GR18D5203 GR18D5204 GR18D5205 GR18D5206	1. Business Analytics 2. Industrial Safety 3. Operations Research 4. Cost Management of Engineering Projects 5. Composite Materials 6. Waste to Energy		-	-	3	30	70	100
3	Dissertation	GR18D5191	Dissertation Phase – I	-	-	20	10	30	70	100
Total				**6**	**-**	**20**	**16**	**90**	**210**	**300**

II YEAR - II SEMESTER

Sl. No	Group	Subject code	Subject	Credits L	Credits T	Credits P	Credits	Int. Marks	Ext. Marks	Total Marks
1	Dissertation	GR18D5192	Dissertation Phase – II	-	-	32	16	30	70	100
Total						32	16	30	70	100

Audit course 1 & 2

Subject Code	Subject Name
GR18D5207	English for Research Paper Writing
GR18D5208	Disaster Management
GR18D5209	Sanskrit for Technical Knowledge
GR18D5210	Value Education
GR18D5211	Indian Constitution
GR18D5212	Pedagogy Studies
GR18D5213	Stress Management by Yoga
GR18D5214	Personality Development through life Enlightenment Skills

GOKARAJU RANGARAJU INSTITUTE OF ENGINEERING AND TECHNOLOGY

DIGITAL SYSTEM DESIGN USING HDL

Course Code: GR18D5076 **L/T/P/C: 3/0/0/3**

Course objectives

- Learn digital design of Sequential Machines.
- Design drawing state graphs.
- Design realization and implementation of SM Charts.
- Design Fault modeling and test pattern generation of Combinational circuits.
- Learn fault diagnosis in sequential circuits and understand machine design, identification of fault detection experiment.

Course outcomes

- Create understanding of the design techniques of sequential Machines.
- Create understanding of the fundamental concepts of PLD's, design of FPGA's.
- Learn implementation of SM charts in combinational and sequential circuits.
- Develop skills in modeling fault free combinational circuits.
- Develop skills in modeling Sequential circuits in terms of reliability, availability and safety.

Unit I: DIGITAL SYSTEM DESIGN AUTOMATION AND RTL DESIGN WITH VERILOG

Digital Design Flow-design entry, Test bench in Verilog, Design validation, Compilation and synthesis, Post synthesis simulation, Timing analysis, Hardware generation in Verilog, Test Benches.

Unit II: VERILOG LANGUAGE CONCEPTS

Characterizing Hardware Languages, Module Basics, Verilog Simulation Model, Compiler Directives, System Tasks and Functions

Unit III: Combinational Circuit Description

Module Wires, Gate Level Logic, Hierarchical Structures, Describing Expressions with Assign statements, Behavioral Combinational Descriptions, Combinational Synthesis

Unit IV: SEQUENTIAL CIRCUIT DESCRIPTION

Sequential models, Basic Memory Components, Functional Registers, State Machine Coding, Sequential Synthesis. Component Test, Verification and Detailed Modeling
Test Bench, Test Bench Techniques, design Verification, Assertion Verification, Text Based Test Benches, Detailed Modeling- Switch Level Modeling, Strength Modeling

Unit V:RTL DESIGN AND TEST

Sequential Multiplier- Shift-and- Add Multiplication process, sequential multiplier design, Multiplier testing, Von Neumann Computer Model- Processor and memory model, processor model specification, designing the adding CPU, Design of data path, Control part design, Adding CPU verilog description, testing adding CPU

Text Books

1. Zainalabdien Navabi, Verlog Digital System Design, TMH, 2nd edition.

Reference Books

1. Fundamentals of Digital Logic with Verilog design by Stephen. Brown and Zvonko Vranesis, TMH, 2nd edition 2010.
2. Digital Logic Design using Verilog, State machine & synthesis for FPGA, Sunggulee, Cengage Learning, 2009
3. Verilog HDL- SamirPalnitkar, 2nd edition.
4. Advanced Digital Design with Verilog HDL- Michael D. Ciletti, PHI, 2005.
5. Digital Systems Design using VHDL- Charles H Roth, Jr. Thomson Publications, 2004

GOKARAJU RANGARAJU INSTITUTE OF ENGINEERING AND TECHNOLOGY

DIGITAL CMOS IC DESIGN

Course Code: GR18D5077 **L/T/P/C: 3/0/0/3**

Course objectives

- To describe over view about evolution of CMOS integrated circuits.
- To provide knowledge about Combinational, Sequential MOS logic circuits
- To introduce and familiarize with the various logic circuits.
- To prepare them to face the challenges in dynamic logic circuits.
- To create interest in the integrated circuit design and prepare them to face .the challenges in VLSI technology.

Course outcomes

- An ability to know about the various Combinational and Sequential MOS logic circuits.
- An in-depth knowledge of applying the concepts on real time applications
- An ability to know the design of dynamic MOS logic circuits.
- Able to know the design of semiconductor memories.
- An ability to understand the basic concepts of Boolean expressions.

Unit I: MOS DESIGN

Pseudo NMOS Logic – Inverter, Inverter threshold voltage, Output high voltage, Output Low voltage, Gain at gate threshold voltage, Transient response, Rise time, Fall time, Pseudo NMOS logic gates, Transistor equivalency, CMOS Inverter logic.

Unit II: COMBINATIONAL MOS LOGIC CIRCUITS

MOS logic circuits with NMOS loads, Primitive CMOS logic gates – NOR & NAND gate, Complex Logic circuits design – Realizing Boolean expressions using NMOS gates and CMOS gates , AOI and OIA gates, CMOS full adder, CMOS transmission gates, Designing with Transmission gates.

Unit III: SEQUENTIAL MOS LOGIC CIRCUITS

Behavior of bistable elements, SR Latch, Clocked latch and flip flop circuits, CMOS D latch and edge triggered flip-flop.

Unit IV: DYNAMIC LOGIC CIRCUITS

Basic principle, Voltage Bootstrapping, Synchronous dynamic pass transistor circuits, Dynamic CMOS transmission gate logic, High performance Dynamic CMOS circuits.

Unit V: SEMICONDUCTOR MEMORIES

Types, RAM array organization, DRAM – Types, Operation, Leakage currents in DRAM cell and refresh operation, SRAM operation Leakage currents in SRAM cells, Flash Memory-NOR flash and NAND flash.

Text Books

1. Digital Integrated Circuit Design – Ken Martin, Oxford University Press, 2011.
2. CMOS Digital Integrated Circuits Analysis and Design – Sung-Mo Kang, Yusuf Leblebici, TMH, 3rd Ed., 2011.

Reference Books

1. Introduction to VLSI Systems: A Logic, Circuit and System Perspective – Ming-BO Lin, CRC Press, 2011
2. Digital Integrated Circuits – A Design Perspective, Jan M. Rabaey, Anantha Chandrakasan, Borivoje Nikolic, 2nd Ed., PHI.

GOKARAJU RANGARAJU INSTITUTE OF ENGINEERING AND TECHNOLOGY
DIGITAL SYSTEM DESIGN

Course Code: GR18D5078 **L/T/P/C: 3/0/0/3**

Course Objectives

- Learn digital design of Sequential Machines.
- Learn drawing state graphs.
- Learn realization and implementation of SM Charts.
- Learn Fault modeling and test pattern generation of Combinational circuits.
- Learn fault diagnosis in sequential circuits and understand machine design, identification of fault detection experiment.

Course Outcomes

- Create understanding of the design techniques of sequential Machines.
- Create understanding of the fundamental concepts of PLD's, design of FPGA's.
- Develop skills in modeling Sequential circuits in terms of reliability, availability and safety.
- Develop skills in modeling fault detection experiments of sequential circuits.

Develop skills in modeling combinational circuits in terms of reliability, availability and safety

Unit I: MINIMIZATION AND TRANSFORMATION OF SEQUENTIAL MACHINES

The Finite State Model – Capabilities and limitations of FSM – State equivalence and machine minimization – Simplification of incompletely specified machines. Fundamental mode model – Flow table – State reduction – Minimal closed covers – Races, Cycles and Hazards.

Unit II: DIGITAL DESIGN

Digital Design Using ROMs, PALs and PLAs, BCD Adder, 32 – bit adder, State graphs for control circuits, Scoreboard and Controller, A shift and add multiplier, Array multiplier, Keypad Scanner, Binary divider.

Unit III: SM CHARTS

State machine charts, Derivation of SM Charts, Realization of SM Chart, Implementation of Binary Multiplier, dice game controller.

Unit IV: FAULT MODELING & TEST PATTERN GENERATION

Logic Fault model – Fault detection & Redundancy- Fault equivalence and fault location – Fault dominance – Single stuck at fault model – Multiple stuck at fault models –Bridging fault model. Fault diagnosis of combinational circuits by conventional methods – Path sensitization techniques, Boolean Difference method – Kohavi algorithm – Test algorithms – D algorithm, PODEM, Random testing, Transition count testing, Signature analysis and test bridging faults.

Unit V: FAULT MODELING & TEST PATTERN GENERATION

Circuit Test Approach, Transition Check Approach – State identification and fault detection experiment, Machine identification, Design of fault detection experiment

Text Books

1. Fundamentals of Logic Design – Charles H. Roth, 5th Ed., Cengage Learning.
2. Digital Systems Testing and Testable Design – Miron Abramovici, Melvin A. Breuer and Arthur D. Friedman- John Wiley & Sons Inc.
3. Logic Design Theory – N. N. Biswas, PHI

Reference Books

1. Switching and Finite Automata Theory – Z. Kohavi , 2nd Ed., 2001, TMH
2. Digital Design – Morris Mano, M.D.Ciletti, 4th Edition, PHI.
3. Digital Circuits and Logic Design – Samuel C. Lee , PHI

GOKARAJU RANGARAJU INSTITUTE OF ENGINEERING AND TECHNOLOGY

DEVICE MODELING

Course Code: GR18D5079 **L/T/P/C: 3/0/0/3**

Course objectives

- To impart to students knowledge of semi conductor physics and integrated passive devices.
- To enable students to analyze the behavior of monolithic diodes with the help of models of integrated diodes.
- To enable students to analyze the behavior of integrated NMOS and PMOS transistors with the help of SPICE models.
- To enable students visualize different VLSI fabrication techniques of different processes.
- To enable students to model hetero junction devices.

Course outcomes

- The graduate student will be equipped with knowledge of semiconductor physics.
- The graduate student will be able relate model parameters to structures of integrated passive devices.
- The graduate will be able to analyze static and dynamic behavior of diodes.
- The graduate student will be able to model electrically NMOS and PMOS transistors.
- The graduate student will be able to use SPICE model level 1, 2,3and 4 and hence will be able to analyze various integrated circuits.

Unit I: INTRODUCTION TO SEMICONDUCTOR PHYSICS

Review of Quantum Mechanics, Boltzman transport equation, Continuity equation, Poisson equation.

Integrated Passive Devices: Types and Structures of resistors and capacitors in monolithic technology, Dependence of model parameters on structures

Unit II: INTEGRATED DIODES

Junction and Schottky diodes in monolithic technologies – Static and Dynamic behavior – Small and large signal models – SPICE models

Integrated Bipolar Transistor: Types and structures in monolithic technologies – Basic model (Eber-Moll) – Gunmel - Poon modeldynamic model, Parasitic effects – SPICE model –Parameter extraction

Unit III: INTEGRATED MOS TRANSISTOR

NMOS and PMOS transistor – Threshold voltage – Threshold voltage equations – MOS device equations – Basic DC equations second order effects – MOS models – small signal AC characteristics – MOS FET SPICE model level 1, 2, 3 and 4

Unit IV: VLSI FABRICATION TECHNIQUES

An overview of wafer fabrication, Wafer Processing – Oxidation –Patterning – Diffusion – Ion Implantation – Deposition – Silicon gate nMOS process – CMOS processes – n-well- p-well- twin tub- Silicon on insulator – CMOS process enhancements –Interconnects circuit elements

Unit V: MODELING OF HETERO JUNCTION DEVICES

Band gap Engineering, Band gap Offset at abrupt Hetero Junction, Modified current continuity equations, Hetero Junction bipolar transistors (HBTs), SiGe

Text Books

1. Introduction to Semiconductor Materials and Devices – Tyagi M. S, 2008, John Wiley Student Edition.
2. Solid State Circuits – Ben G. Streetman, Prentice Hall, 1997

Reference Books

1. Physics of Semiconductor Devices – Sze S. M, 2nd Edition, Mcgraw Hill, New York, 1981.
2. Introduction to Device Modeling and Circuit Simulation – Tor A. Fijedly, Wiley-Interscience, 1997.

GOKARAJU RANGARAJU INSTITUTE OF ENGINEERING AND TECHNOLOGY

SCRIPTING LANGUAGES FOR VLSI

Course Code: GR18D5080 **L/T/P/C: 3/0/0/3**

Course objectives

- To describe the need of using scripting language programs.
- To use PERL scripting language at the instances required.
- To apply advanced level PERL for software automation.
- To employ the PERL scripting language for file system navigation.
- To illustrate software automation using TCL

Course outcomes

- The students will be in a position to judge whether scripting language program is needed for a particular code.
- Students will be acquainted with the basic level scripting language programming in PERL.
- Students will be skillful to code in PERL for advanced level software automation.
- Students will have the programming skills to automate the software for event-driven programs too.
- Students will be in a position to demonstrate software automation using Java Script, PERL-TK, and in basic level using python scripting language.

Unit I: INTRODUCTION TO SCRIPTS AND SCRIPTING

Characteristics and uses of scripting languages, Introduction to PERL, Names and values, Variables and assignment, Scalar expressions, Control structures, Built-in functions, Collections of Data, Working with arrays, Lists and hashes, Simple input and output, Strings, Patterns and regular expressions, Subroutines, Scripts with arguments.

Unit II: ADVANCED PERL

Finer points of looping, subroutines, using pack and unpack, working with files, navigating the file system, type globs, eval, references, data structures, packages, libraries and modules, objects, objects and modules in action, tied variables, interfacing to the operating systems, security issues.

Unit III: TCL

The TCL phenomena, Philosophy, Structure, Syntax, Parser, Variables and data in TCL, Control flow, Data structures, Simple input/output, Procedures, Working with Strings, Patterns, Files and Pipes, Example code.

Unit IV: ADVANCED TCL

The eval, source, exec and up-level commands, Libraries and packages, Namespaces, Trapping errors, Event-driven programs, Making applications 'Internet-aware', 'Nuts-and-bolts' internet programming, Security issues, running untrusted code, The C interface.

Unit V: TK AND JAVASCRIPT

Visual tool kits, Fundamental concepts of TK, TK by example, Events and bindings, Geometry managers, PERL-TK. JavaScript – Object models, Design Philosophy, Versions of JavaScript, The Java Script core language, Basic concepts of Python.
Object Oriented Programming Concepts (Qualitative Concepts Only): Objects, Classes, Encapsulation, Data Hierarchy.

Text Books

1. The World of Scripting Languages- David Barron, Wiley Student Edition, 2010.
2. Practical Programming in Tcl and Tk - Brent Welch, Ken Jones and Jeff Hobbs., Fourth edition.
3. Java the Complete Reference - Herbert Schildt, 7th Edition, TMH.

Reference Books

1. Tcl/Tk: A Developer's Guide- Clif Flynt, 2003, Morgan Kaufmann SerieS.
2. Tcl and the Tk Toolkit- John Ousterhout, 2nd Edition, 2009, Kindel Edition.

GOKARAJU RANGARAJU INSTITUTE OF ENGINEERING AND TECHNOLOGY

CPLD AND FPGA ARCHITECURES

Course Code: GR18D5081 **L/T/P/C: 3/0/0/3**

Course objectives

- To understand the concept of Programmable Logic Device architectures and technologies.
- Underlying FPGA architectures and technologies in detail.
- To understand the difference between CPLDs and FPGAs.
- To provide knowledge about SRAM Programmable FPGA Device architecture.
- To comprehend knowledge about Anti-Fuse Programmable FPGA Device architecture.

Course outcomes

- To know the concept of program able architectures.
- Perceiving CPLD and FPGA technologies.
- Study and compare the different architectures of CPLDs and FPGAs.
- An ability to know the SRAM Technology based FPGAs.
- An ability to know the Anti-Fuse Technology based FPGAs

Unit I: INTRODUCTION TO PROGRAMMABLE LOGIC DEVICES

Introduction, Simple Programmable Logic Devices – Read Only Memories, Programmable Logic Arrays, Programmable Array Logic, Programmable Logic Devices/Generic Array Logic; Complex Programmable Logic Devices – Architecture of Xilinx Cool Runner XCR3064XL CPLD, CPLD Implementation of a Parallel Adder with Accumulation.

Unit II: FIELD PROGRAMMABLE GATE ARRAYS

Organization of FPGAs, FPGA Programming Technologies, Programmable Logic Block Architectures, Programmable Interconnects, Programmable I/O blocks in FPGAs, Dedicated Specialized Components of FPGAs, Applications of FPGAs.

Unit III: SRAM PROGRAMMABLE FPGAS

Introduction, Programming Technology, Device Architecture, The Xilinx XC2000, XC3000 and XC4000 Architectures.

Unit IV: ANTI-FUSE PROGRAMMED FPGAS

Introduction, Programming Technology, Device Architecture, The Actel ACT1, ACT2 and ACT3 Architectures.

Unit V: DESIGN APPLICATIONS

General Design Issues, Counter Examples, A Fast Video Controller, A Position Tracker for a Robot Manipulator, A Fast DMA Controller, Designing Counters with ACT devices, Designing Adders and Accumulators with the ACT Architecture.

Text Books

1. Field Programmable Gate Array Technology - Stephen M. Trimberger, Springer International Edition.
2. Digital Systems Design - Charles H. Roth Jr, Lizy Kurian John, Cengage Learning.

Reference Books

1. Field Programmable Gate Arrays - John V. Oldfield, Richard C. Dorf, Wiley India.
2. Digital Design Using Field Programmable Gate Arrays - Pak K. Chan/Samiha Mourad, Pearson Low Price Edition.
3. Digital Systems Design with FPGAs and CPLDs - Ian Grout, Elsevier, Newnes.
4. FPGA based System Design - Wayne Wolf, Prentice Hall Modern Semiconductor Design Series.

GOKARAJU RANGARAJU INSTITUTE OF ENGINEERING AND TECHNOLOGY

MICROCONTROLLERS FOR EMBEDDED SYSTEMS

Course Code: GR18D5082 **L/T/P/C: 3/0/0/3**

Course objectives

- To introduce the outline architecture of ARM7 microcontroller including basics of pipelines, registers, exception modes.
- To set up and customize a microcontroller development environment.
- To give an overview of system peripherals which cover bus structure, memory map, register programming and much more.
- To write programs that interact with other devices.
- To learn the Memory Management of RISC Microcontrollers.

Course outcomes

- An ability to understand the hardware implementation of the ARM7microcontrollers.
- An ability to integrate peripherals based on I/O functions.
- An ability to learn the concept of pipelines, registers and exception modes.
- An ability to program in ARM and THUMB modes.
- An ability to interpret the functions of Memory Management Unit (MMU).

Unit I: ARM ARCHITECTURE

ARM Design Philosophy, Registers, Program Status Register, Instruction Pipeline, Interrupts and Vector Table, Architecture Revision, ARM Processor Families.

Unit II: ARM PROGRAMMING MODEL – I

Instruction Set: Data Processing Instructions, Addressing Modes, Branch, Load, Store Instructions, PSR Instructions, Conditional Instructions.

Unit III: ARM PROGRAMMING MODEL – II

Thumb Instruction Set: Register Usage, Other Branch Instructions, Data Processing Instructions, Single-Register and Multi Register Load-Store Instructions, Stack, Software Interrupt Instructions

Unit IV: ARM PROGRAMMING

Simple C Programs using Function Calls, Pointers, Structures, Integer and Floating Point Arithmetic, Assembly Code using Instruction Scheduling, Register Allocation, Conditional Execution and Loops.

Unit V: MEMORY MANAGEMENT

Cache Architecture, Polices, Flushing and Caches, MMU, Page Tables, Translation, Access Permissions, Context Switch.

Text Books

1. ARM Systems Developer's Guides- Designing & Optimizing System Software – Andrew N. Sloss, Dominic Symes, Chris Wright, 2008, Elsevier.

Reference Books

1. Embedded Microcomputer Systems, Real Time Interfacing – Jonathan W. Valvano – Brookes / Cole, 1999, Thomas Learning.

GOKARAJU RANGARAJU INSTITUTE OF ENGINEERING AND TECHNOLOGY

VLSI TECHNOLOGY AND DESIGN

Course Code: GR18D5083 **L/T/P/C: 3/0/0/3**

Course objectives

- To enable the student to visualize MOS fabrication technologies and to understand electrical properties of MOS, CMOS and Bi CMOS circuits.
- To train the student to draw integrated circuit layouts following design rules.
- To enable the student design combinational circuit, do verification, power optimization and network testing.
- To enable the student to use power optimization techniques, design validation procedures and testing of sequential circuits.
- To train the student to use different floor planning methods and different low power architectures.

Course outcomes

- Visualize the steps taken for MOS fabrication technologies.
- Analyze electrical behavior of MOS, CMOS and Bi CMOS circuits.
- Draw the layout of integrated circuits following design rules.
- Design combinational circuit.
- Design sequential circuits using different clocking disciplines.

Unit I: REVIEW OF MICROELECTRONICS AND INTRODUCTION TO MOS TECHNOLOGIES

MOS, CMOS, BiCMOS Technology. Basic Electrical Properties of MOS, CMOS & BiCMOS Circuits: Ids – Vds relationships, Threshold Voltage VT, Gm, Gds and ωo, Pass Transistor, MOS, CMOS & Bi CMOS Inverters, Zpu/Zpd, MOS Transistor circuit model, Latch-up in CMOS circuits.

Unit II: LAYOUT DESIGN AND TOOLS

Transistor structures, Wires and Vias, Scalable Design rules, Layout Design tools.
Logic Gates & Layouts: Static Complementary Gates, Switch Logic, Alternative Gate circuits, Low power gates, Resistive and Inductive interconnect delays.

Unit III: COMBINATIONAL LOGIC NETWORKS

Layouts, Simulation, Network delay, Interconnect design, Power optimization, Switch logic networks, Gate and Network testing.

Unit IV: SEQUENTIAL SYSTEMS

Memory cells and Arrays, Clocking disciplines, Design, Power optimization, Design validation and testing.

Unit V: SEQUENTIAL SYSTEMS

Sequential Systems: Floor planning methods, Global Interconnect, Floor Plan Design, Off-chip connections.

Text Books

1. Essentials of VLSI Circuits and Systems, K. Eshraghian Eshraghian. D, A. Pucknell, 2005, PHI.
2. Modern VLSI Design – Wayne Wolf, 3rd Ed., 1997, Pearson Education.

Reference Books

1. Introduction to VLSI Systems: A Logic, Circuit and System Perspective – Ming-BO Lin, CRCPress, 2011.
2. Principals of CMOS VLSI Design – N.H.E Weste, K. Eshraghian, 2nd Ed., AddisonWesley.

GOKARAJU RANGARAJU INSTITUTE OF ENGINEERING AND TECHNOLOGY

HDL SIMULATION LAB

Course Code: GR18D5084 **L/T/P/C: 0/0/4/2**

Course objectives

This lab deals with programming using Verilog for advanced digital design techniques. It offers board coverage of HDL from a practical design perspective. Introduces students to gate, dataflow(RTL) and behavioral modeling.

Note: All the following digital circuits are to be designed and implemented on FPGA using XILINX's/ Altera's/ Equivalent CAD tools.

Programming can be done using any HDL compiler, Verification of the Functionality of the module using functional Simulator, Timing Simulator for Critical Path tine Calculation, Synthesis of module, Place & Route and implementation of design using FPGA.

Task1

Digital Circuits Description using Verilog/ VHDL

Task2

Verification of the Functionality of designed Circuits using function Simulator.

Task3

Timing Simulation for critical path time calculation.

Task4

Synthesis of Digital Circuits.

Task5

Place and Route techniques for major FPGA vendors such as Xilinx/ Altera/ Actel etc.

Task6

Implementation of Designed Digital Circuits using FPGA and CPLD devices.

GOKARAJU RANGARAJU INSTITUTE OF ENGINEERING AND TECHNOLOGY

DIGITAL CMOS IC DESIGN LAB

Course Code: GR18D5085 **L/T/P/C: 0/0/4/2**

Course objectives

- To describe over view about evolution of CMOS integrated circuits.
- To provide knowledge about Combinational, Sequential MOS logic circuits
- To introduce and familiarize with the various logic circuits.
- To prepare them to face the challenges in dynamic logic circuits.
- To prepare them to design various building blocks in combinational and sequential circuits.

Course outcomes

- An ability to know about the various Combinational and Sequential MOS logic circuits.
- An in-depth knowledge of applying the concepts on real time applications
- An ability to understand the basic concepts of Boolean expressions.
- Able to design different Combinational logic blocks.
- Able to analyze and implement various memory elements.

Task1

For a given specifications plot the characteristics for NMOS and PMOS transistors by varying $I_{D,}$ V_{DS} and V_{GS}.

Task2

For a given specifications plot VTC Curve for CMOS Inverter and calculate $V_{IL,}$ $V_{IH,}$ $NM_{H,}$ $NM_{L.}$

Task3

For a given specifications plot VTC Curve for CMOS Inverter with varying VDD

Task4

For a given specifications plot VTC Curve for CMOS Inverter with varying Device size.

Task5

Perform transient of CMOS inverter with no0 load and with load and determine T_{PHL}, $T_{P}HL$.

Task6

Design and Draw layout for CMOS NOR/ NAND gate and perform DRC, LVS, RC Extraction.

Task7

Design and Draw layout for CMOS XOR gate using Transmission Gates and perform DRC, LVS, RC Extraction.

Task8

Design and Draw layout for combinational function using CMOS logic and perform DRC, LVS, RC Extraction.

Task9

Design and Draw layout for D- Flip Flop using CMOS logic and perform DRC, LVS, RC Extraction.

Note: All the following digital circuits are to be designed and implemented using Cadence/ Mentor Graphics/ Synopsys/ equivalent CAD Tools.

GOKARAJU RANGARAJU INSTITUTE OF ENGINEERING AND TECHNOLOGY

ANALOG CMOS IC DESIGN

Course Code: GR18D5086 **L/T/P/C: 3/0/0/3**

Course objectives

- To describe over view about evolution of CMOS integrated circuits.
- To provide knowledge about fabrication process and technology.
- To introduce and familiarize with the various Amplifiers &OP-amps.
- To prepare them to face the challenges in CMOS technology.
- To design the various comparators and characterize.

Course outcomes

- Able to develop an in-depth understanding of the design principles and applications of CMOS analog IC design.
- An ability to know the fabrication steps involved in CMOS technology.
- Familiar with the small signal and large signal models of CMOS transistors.
- An in-depth knowledge of applying the concepts on real time applications.
- Analyze and design of CMOS op Amps and compensation techniques.

UNIT I: MOS DEVICES AND MODELING

The MOS Transistor, Passive Components- Capacitor & Resistor, Integrated circuit Layout, CMOS Device Modeling - Simple MOS Large-Signal Model, Other Model Parameters, Small-Signal Model for the MOS Transistor, Computer Simulation Models, Sub-threshold MOS Model.

UNIT II: ANALOG CMOS SUB-CIRCUITS

MOS Switch, MOS Diode, MOS Active Resistor, Current Sinks and Sources, Current Mirrors-Current mirror with Beta Helper, Degeneration, Cascode current Mirror and Wilson Current Mirror, Current and Voltage References, Band gap Reference.

UNIT III: CMOS AMPLIFIERS

Inverters, Differential Amplifiers, Cascode Amplifiers, Current Amplifiers, Output Amplifiers, High Gain Amplifiers Architectures.

UNIT IV: CMOS OPERATIONAL AMPLIFIERS

Design of CMOS Op Amps, Compensation of Op Amps, Design of Two-Stage Op Amps, Power-Supply Rejection Ratio of Two-Stage Op Amps, Cascode Op Amps, Measurement Techniques of OP Amp.

UNIT V: COMPARATORS

Characterization of Comparator, Two-Stage, Open-Loop Comparators, Other Open-Loop Comparators, Improving the Performance of Open-Loop Comparators, Discrete-Time Comparators.

TEXT BOOKS

1. CMOS Analog Circuit Design - Philip E. Allen and Douglas R. Holberg, Oxford University Press, International Second Edition/Indian Edition, 2010.
2. Analysis and Design of Analog Integrated Circuits- Paul R. Gray, Paul J. Hurst, S. Lewis and R. G. Meyer, Wiley India, Fifth Edition, 2010.

REFERENCE BOOKS

1. Analog Integrated Circuit Design- David A. Johns, Ken Martin, Wiley Student Edn, 2013.
2. Design of Analog CMOS Integrated Circuits- Behzad Razavi, TMH Edition.
3. CMOS: Circuit Design, Layout and Simulation- Baker, Li and Boyce, PHI.

GOKARAJU RANGARAJU INSTITUTE OF ENGINEERING AND TECHNOLOGY

ASIC DESIGN

Course Code: GR18D5087 **L/T/P/C: 3/0/0/3**

Course objectives

- To understand the ASICs and CMOS logic.
- To learn the various synthesis and static timing analysis.
- To learn the implementation design for testability.
- To understand concept of routing techniques.
- To understand the latest design techniques as practiced in the Industry for design layout optimization.

Course outcomes

- Apply the appropriate design practices, software tools, and research methods for IC design.
- Design the systems by using synthesis and static timing analysis.
- Design the low power digital systems by applying appropriate partitioning and Floor planning algorithms.
- Design the real time applications using routing techniques.
- Understand the concepts of geometric programming and convex functions.

Unit I: INTRODUCTION TO ASIC'S AND CMOS LOGIC

Types of ASICs - Design flow - CMOS transistors - CMOS Design rules - Combinational Logic Cell –Sequential logic cell - Data path logic cell-Transistors as Resistors - Transistor Parasitic Capacitance- Logical effort.

ASIC Library Design and Programmable Technologies

Library cell design - Schematic view of Library architecture - Anti fuse - Static RAM - EPROM and EEPROM technology - PREP benchmarks

Unit II: ASIC VERIFICATION

The Verification Process, The Verification Methodology Manual, Basic Testbench Functionality, Methodology Basics, Constrained-Random Stimulus, Functional Coverage, Testbench Components, Building a Layered Testbench, Simulation Environment Phases, Maximum Code Reuse, Testbench Performance

Unit III: SYNTHESIS AND STATIC TIMING ANALYSIS

Logic Simulation – Types of Simulation – Synthesis: RTL and Technology Schematics-Schematic entry Needs for testing – Types of testing - Boundary scan test - Fault simulation - Automatic test pattern generation. Logic Synthesis and Optimization. Design levels. Main concepts. Basic steps of synthesis. Logic synthesis. Specification. Design description. Design constraints. Logic circuit. Logic synthesis steps. Parameter trade-off. Cell logic model. Characterization, Timing and Area Constraints. Static Timing Analysis(STA)-Need of STA at Different Design Phases and Limitations.

Unit IV: DESIGN FOR TESTABILITY

Challenges of DFT. Quality achievement problems. Systematic defects. Stuck-at fault model. Undetectable faults. Test coverage and fault coverage. Testing sequential designs. Scannable equivalent flip-flop. Scan testing protocol: example. Overlap of test patterns. Scannable equivalent flip-flop. Ripple-counter violation. Ripple-counter RTL DFT solution. Physical-aware DFT flow. SCANDEF file. Re-ppartitioning with SCANDEF. Alpha-numeric ordering. Reordering within scan chain. Reordering across scan-chains. Clock tree based reordering. Placement-based scan chain routing. Increase of power consumption by scan testings.

Unit V: PHYSICAL DESIGN

Physical design flow, System partition -Partitioning methods - Floor planning - Placement -– Global routing - Detailed routing - Circuit extraction – DRC.

Text Books

1. M.J.S .Smith, "Application Specific Integrated Circuits", Pearson Education, 2010.
2. Farzad Nekoogar and FaranakNekoogar, "From ASICs to SOCs: A Practical Approach", Prentice Hall PTR, 2003.
D. Papa, I. Markov. "Multi-Objective Optimization in Physical Synthesis of Integrated Circuits" Springer; 2012.
4.V.Taraate, "Digital Logic Design Using Verilog: Coding and RTL Synthesis", Springer; 2016.

Reference Books

1. G.Hachtel, F. Somenzi. Logic Synthesis and Verification Algorithms. Springer; 2013
2. Digital Design Using Field Programmable Gate Arrays - Pak K. Chan/Samiha Mourad, Pearson Low Price Edition

GOKARAJU RANGARAJU INSTITUTE OF ENGINEERING AND TECHNOLOGY

OPTIMIZATION TECHNIQUES IN VLSI DESIGN

Course Code: GR18D5088 **L/T/P/C: 3/0/0/3**

Course objectives

- To understand the tradeoffs among various design styles given a set of design constraints in physical design automation and to understand performance/area tradeoffs in a chip design process.
- To learn the various statistic modeling methods like Monte Carlo techniques and Pelgroms model etc.,
- To learn the implementation issues for digital design automation including optimization techniques.
- To understand concept of design optimization algorithms and their application to physical design automation.
- To understand the latest design techniques as practiced in the Industry for design layout optimization.

Course outcomes

- Apply the appropriate design practices, emerging technologies, state-of-the-art design techniques, software tools, and research methods for IC design.
- Design the systems by using concepts of High level statistical, Gate level statistical analysis methods.
- Design the low power digital systems by applying appropriate partitioning and Floor planning algorithms.
- Design the real time applications using optimization techniques like Genetic Algorithms.
- Understand the concepts of geometric programming and convex functions.

Unit I: STATISTICAL MODELING

Modeling sources of variations, Monte Carlo techniques, Process variation modeling-Pelgroms model, Principle component based modeling, Quad tree based modeling, Performance modeling-Response surface methodology, delay modeling, interconnect delay models.

Unit II: STATISTICAL PERFORMANCE, POWER AND YIELD ANALYSIS

Statistical timing analysis, parameter space techniques, Bayesian networks Leakage models, High level statistical analysis, Gate level statistical analysis, dynamic power, leakage power, temperature and power supply variations, High level yield estimation and gate level yield estimation.

Unit III: CONVEX OPTIMIZATION

Convex sets, convex functions, geometric programming, trade-off and sensitivity analysis, Generalized geometric programming, geometric programming applied to digital circuit gate sizing, Floor planning, wire sizing, Approximation and fitting- Monomial fitting, Maxmonomial fitting, Posynomial fitting.

Unit IV: GENETIC ALGORITHM

Introduction, GA Technology-Steady State Algorithm-Fitness Scaling-Inversion GA for VLSI Design, Layout and Test automation- partitioning-automatic placement, routing technology, Mapping for FPGA- Automatic test generation- Partitioning algorithm Taxonomy-Multi-way Partitioning Hybrid genetic-encoding-local improvement-WDFR Comparison of CAS-Standard cell placement-GASP algorithm-unified algorithm.

Unit V: GA ROUTING PROCEDURES AND POWER ESTIMATION:

Global routing-FPGA technology mapping-circuit generation-test generation in a GA frame work-test generation procedures, Power estimation-application of GA-Standard cell placement-GA for ATGproblem encoding- fitness function-GA Vs Conventional algorithm.

Text Books / Reference Books

1. Statistical Analysis and Optimization for VLSI: Timing and Power - Ashish Srivastava, Dennis Sylvester, David Blaauw, Springer, 2005.
2. Genetic Algorithm for VLSI Design, Layout and Test Automation - Pinaki Mazumder, E.Mrudnick, Prentice Hall,1998.
3. Convex Optimization - Stephen Boyd, Lieven Vandenberghe, Cambridge University Press, 2004.

GOKARAJU RANGARAJU INSTITUTE OF ENGINEERING AND TECHNOLOGY
SYSTEM ON CHIP ARCHITECTURE

Course Code: GR18D5089 **L/T/P/C: 3/0/0/3**

Course objectives

- To describe the system design approach with respect to the hardware and software.
- To apply the techniques for reducing the delays in program execution.
- To categorize and compare different processor types for their selection into a System on Chip.
- To compare different memory designs and their purposes
- To interpret the architectures and applications of various buses.

Course outcomes

- Students will be able to summarize all the components required for system design.
- Students will be acquired the techniques to minimize the delays for better performance of a system on chip.
- Students will be able to analyze different types of buses for respective applications.
- Students will be skilful to judge a configurable device based on the application requirement for a system onchip
- Students will have the technique to implement AES algorithm if required.

Unit I: INTRODUCTION TO THE SYSTEM APPROACH

System Architecture, Components of the system, Hardware & Software, Processor Architectures, Memory and Addressing. System level interconnection, An approach for SOC Design, System Architecture and Complexity.

Unit II: PROCESSORS

Introduction , Processor Selection for SOC, Basic concepts in Processor Architecture, Basic concepts in Processor Micro Architecture, Basic elements in Instruction handling. Buffers: minimizing Pipeline Delays, Branches, More Robust Processors, Vector Processors and Vector Instructions extensions, VLIW Processors, Superscalar Processors.

Unit III: MEMORY DESIGN FOR SOC

Overview of SOC external memory, Internal Memory, Size, Scratchpads and Cache memory, Cache Organization, Cache data, Write Policies, Strategies for line replacement at miss time, Types of Cache, Split – I, and D – Caches, Multilevel Caches, Virtual to real translation , SOC Memory System, Models of Simple Processor – memory interaction.

Unit IV: INTERCONNECT CUSTOMIZATION AND CONFIGURATION

Inter Connect Architectures, Bus: Basic Architectures, SOC Standard Buses, Analytic Bus Models, Using the Bus model, Effects of Bus transactions and contention time. SOC Customization: An overview, Customizing Instruction Processor, Reconfiguration Technologies, Mapping design onto Reconfigurable devices, Instance- Specific design, Customizable Soft Processor, Reconfiguration -overhead analysis and trade-off analysis on reconfigurable Parallelism.

Unit V: APPLICATION STUDIES / CASE STUDIES

SOC Design approach, AES algorithms, Design and evaluation, Image compression – JPEG Compression.

Text Books

1. Computer System Design System-on-Chip - Michael J. Flynn and Wayne Luk, Wiely India Pvt. Ltd.
2. ARM System on Chip Architecture – Steve Furber –2nd Ed., 2000, Addison Wesley Professional

Reference Books

1. Design of System on a Chip: Devices and Components – Ricardo Reis, 1st Ed., 2004, Springer
2. Co-Verification of Hardware and Software for ARM System on Chip Design (Embedded Technology) – Jason Andrews – Newnes, BK and CDROM

GOKARAJU RANGARAJU INSTITUTE OF ENGINEERING AND TECHNOLOGY
DESIGN FOR TESTABILITY

Course Code: GR18D5090 **L/T/P/C: 3/0/0/3**

Course objectives

- To provide knowledge about VLSI Testing.
- To understand VLSI Technology Trends affecting Testing
- To get knowledge on Design verification and Test Evaluation
- To understand the concept of BIST architecture.
- To provide knowledge about Boundary Scan Test.

Course outcomes

- Create understanding of the fundamental concepts of Testing in VLSI design.
- Perceiving Trends affecting Testing.
- An ability to know the high level testability measures and scan methods.
- An ability to know the BIST architecture: Test pattern generation, Circuit under test and Output response analyzer.
- Develop skills in modeling and evaluating Boundary Scan Standards.

Unit I: INTRODUCTION TO TESTING

Testing Philosophy, Role of Testing, Digital and Analog VLSI Testing, VLSI Technology Trends affecting Testing, Types of Testing, Fault Modeling: Defects, Errors and Faults, Functional Versus Structural Testing, Levels of Fault Models, Single Stuck-at Fault.

Unit II: LOGIC AND FAULT SIMULATION

Simulation for Design Verification and Test Evaluation, Modeling Circuits for Simulation, Algorithms for True-value Simulation, Algorithms for Fault Simulation, ATPG.

Unit III: TESTABILITY MEASURES

SCOAP Controllability and Observability, High Level Testability Measures, Digital DFT and Scan Design: Ad-Hoc DFT Methods, Scan Design, Partial-Scan Design, Variations of Scan.

Unit IV: BUILT-IN SELF-TEST

The Economic Case for BIST, Random Logic BIST: Definitions, BIST Process, Pattern Generation, Response Compaction, Built-In Logic Block Observers, Test-Per-Clock, Test-Per-Scan BIST Systems, Circular Self Test Path System, Memory BIST, Delay Fault BIST.

Unit V: BOUNDARY SCAN STANDARD

Motivation, System Configuration with Boundary Scan: TAP Controller and Port, Boundary Scan Test Instructions, Pin Constraints of the Standard, Boundary Scan Description Language: BDSL Description Components, Pin Descriptions.

Text Books

1. Essentials of Electronic Testing for Digital, Memory and Mixed Signal VLSI Circuits - M.L. Bushnell, V. D. Agrawal, Kluwer Academic Pulishers.

Reference Books

1. Digital Systems and Testable Design - M. Abramovici, M.A.Breuer and A.D Friedman, Jaico Publishing House.
2. Digital Circuits Testing and Testability - P.K. Lala, Academic Press.

GOKARAJU RANGARAJU INSTITUTE OF ENGINEERING AND TECHNOLOGY

DIGITAL SIGNAL PROCESSORS AND ARCHITECTURE

Course Code: GR18D5091 **L/T/P/C: 3/0/0/3**

Course objectives

- To provide sound foundation of digital signal processing (DSP) architectures for designing efficient VLSI architectures for DSP systems.
- To analyze general purpose digital signal processors.
- To understand pipelining, parallel processing and retiming.
- To illustrate the features of on-chip peripheral devices and its interfacing along with its programming details.
- To analyze DSP architectures.

Course outcomes

- An ability to recognize the fundamentals of fixed and floating point architectures of various DSPs.
- An ability to learn the architecture details and instruction sets of fixed and floating point DSPs.
- An ability to Infer about the control instructions, interrupts, and pipeline operations.
- Anabilitytoanalyzeandlearntoimplementthesignalprocessingalgorithmsin DSPs.
- An ability to learn the DSP programming tools and use them for applications.

Unit I: INTRODUCTION TO DIGITAL SIGNAL PROCESSING

Introduction, a Digital signal-processing system, the sampling process, discrete time sequences. Discrete Fourier Transform (DFT) and Fast Fourier Transform (FFT), Linear time-invariant systems, Digital filters, Decimation and interpolation.

Unit II: COMPUTATIONAL ACCURACY IN DSP IMPLEMENTATIONS

Number formats for signals and coefficients in DSP systems, Dynamic Range and Precision, Sources of error in DSP implementations, A/D Conversion errors, DSP Computational errors, D/A Conversion Errors, Compensating filter.

Unit III: ARCHITECTURES FOR PROGRAMMABLE DSP DEVICES

Basic Architectural features, DSP Computational Building Blocks, Bus Architecture and Memory, Data Addressing Capabilities, Address Generation UNIT, Programmability and Program Execution, Speed Issues, Features for External interfacing.

Unit IV: PROGRAMMABLE DIGITAL SIGNAL PROCESSORS

Commercial Digital signal-processing Devices, Data Addressing modes of TMS320C54XX DSPs, Data Addressing modes of TMS320C54XX Processors, Memory space of TMS320C54XX Processors, Program Control, TMS320C54XX Instructions and Programming, On-Chip Peripherals, Interrupts of TMS320C54XX Processors, Pipeline Operation of TMS320C54XX Processors.

Unit V: ANALOG DEVICES FAMILY OF DSP DEVICES

Analog Devices Family of DSP Devices – ALU and MAC block diagram, Shifter Instruction, Base Architecture of ADSP 2100, ADSP-2181 high performance Processor. Introduction to Black fin Processor - The Black fin Processor, Introduction to Micro Signal Architecture,

Overview of Hardware Processing Units and Register files, Address Arithmetic Unit, Control Unit, Bus Architecture and Memory, Basic Peripherals.

Text Books

1. Digital Signal Processing – Avtar Singh and S. Srinivasan, Thomson Publications, 2004.
2. A Practical Approach To Digital Signal Processing - K Padmanabhan, R. Vijayarajeswaran, Ananthi. S, New Age International, 2006/2009
3. Embedded Signal Processing with the Micro Signal Architecture: Woon-Seng Gan, Sen M. Kuo, Wiley-IEEE Press, 2007

Reference Books

1. Digital Signal Processors, Architecture, Programming and Applications – B. Venkataramani and M. Bhaskar, 2002, TMH.
2. Digital Signal Processing – Jonatham Stein, 2005, John Wiley.

GOKARAJU RANGARAJU INSTITUTE OF ENGINEERING AND TECHNOLOGY

LOW POWER VLSI DESIGN

Course Code: GR18D5092 **L/T/P/C: 3/0/0/3**

Course objectives

- To know about the need for low power circuit design.
- To provide strong foundation of fundamentals of low power circuit design.
- To furnish knowledge of various low power design approaches for VLSI System design.
- To analyze different low power design techniques.
- To develop different low voltage low power logic styles using low power techniques.

COURSE OUTCOMES

- Student develops strong knowledge of fundamentals of low power VLSI circuit design.
- Student will be aware of various low power VLSI design approaches.
- Student will be aware of various low power logic styles.
- Student will be able to analyze all the low power design techniques.
- Student will develop the capability of designing low power data path subsystems such as adders and multipliers.

Unit I: FUNDAMENTALS

Need for Low Power Circuit Design, Sources of Power Dissipation – Switching Power Dissipation, Short Circuit Power Dissipation, Leakage Power Dissipation, Glitching Power Dissipation, Short Channel Effects –Drain Induced Barrier Lowering and Punch Through, Surface Scattering, Velocity Saturation, Impact Ionization, Hot Electron Effect.

Unit II: LOW-POWER DESIGN APPROACHES

Low-Power Design through Voltage Scaling – VTCMOS circuits, MTCMOS circuits, Architectural Level Approach –Pipelining and Parallel Processing Approaches.
Switched Capacitance Minimization Approaches:
System Level Measures, Circuit Level Measures, Mask level Measures.

Unit III: LOW-VOLTAGE LOW-POWER ADDERS

Introduction, Standard Adder Cells, CMOS Adder's Architectures – Ripple Carry Adders, Carry Look-Ahead Adders, Carry Select Adders, Carry Save Adders, Low-Voltage Low-Power Design Techniques –Trends of Technology and Power Supply Voltage, Low-Voltage Low-Power Logic Styles.

Unit IV: LOW-VOLTAGE LOW-POWER MULTIPLIERS

Introduction, Overview of Multiplication, Types of Multiplier Architectures, Braun Multiplier, Baugh-Wooley Multiplier, Booth Multiplier, Introduction to Wallace Tree Multiplier.

Unit V: LOW-VOLTAGE LOW-POWER MEMORIES

Basics of ROM, Low-Power ROM Technology, Future Trend and Development of ROMs, Basics of SRAM, Memory Cell, Precharge and Equalization Circuit, Low-Power SRAM Technologies, Basics of DRAM, Self-Refresh Circuit, Future Trend and Development of DRAM.

Text Books

1. CMOS Digital Integrated Circuits – Analysis and Design – Sung-Mo Kang, Yusuf Leblebici, TMH, 2011.
2. Low-Voltage, Low-Power VLSI Subsystems – Kiat-Seng Yeo, Kaushik Roy, TMH Professional Engineering.

Reference Books

1. Introduction to VLSI Systems: A Logic, Circuit and System Perspective – Ming-BO Lin, CRC Press, 2011
2. Low Power CMOS Design – AnanthaChandrakasan, IEEE Press/Wiley International, 1998.

GOKARAJU RANGARAJU INSTITUTE OF ENGINEERING AND TECHNOLOGY
HARDWARE SOFTWARE CO-DESIGN

Course Code: GR18D5093 **L/T/P/C: 3/0/0/3**

Course objectives

- Describeanembeddedsystemdesignflowfromspecificationtophysicalrealization
- Describe structural behavior of systems.
- Master complex systems.
- Devise new theories, techniques, and tools in design, implementation and testing.
- Master contemporary development techniques.

Course outcomes

- Gain knowledge of contemporary issues and algorithms used.
- Know the interfacing components, different verification techniques and tools.
- Demonstrate practical skills in the construction of prototypes.
- Understand the use of modern hardware and software tools for building prototypes of embedded systems.
- Apply embedded software techniques to satisfy functional and response time requirements.

Unit I: CO- DESIGN ISSUES

Co- Design Models, Architectures, Languages, A Generic Co-design Methodology.
Co- Synthesis Algorithms: Hardware software synthesis algorithms: hardware – software partitioning distributed system co-synthesis.

Unit II: PROTOTYPING AND EMULATION

Prototyping and emulation techniques, prototyping and emulation environments, future developments in emulation and prototyping architecture specialization techniques, system communication infrastructure

Target Architectures:

Architecture Specialization techniques, System Communication infrastructure, Target Architecture and Application System classes, Architecture for control dominated systems (8051-Architectures for High performance control), Architecture for Data dominated systems (ADSP21060, TMS320C60), Mixed Systems.

Unit III: COMPILATION TECHNIQUES AND TOOLS FOR EMBEDDED PROCESSOR ARCHITECTURES

Modern embedded architectures, embedded software development needs, compilation technologies, practical consideration in a compiler development environment.

Unit IV: DESIGN SPECIFICATION AND VERIFICATION

Design, co-design, the co-design computational model, concurrency coordinating concurrent Computations, interfacing components, design verification, implementation verification, verification tools, interface verification

Unit V

Languages for System – Level Specification and Design-I:

System – level specification, design representation for system level synthesis, system level specification languages,

Languages for System – Level Specification and Design-II:

Heterogeneous specifications and multi language co-simulation, the cosyma system and lycos system.

Text Books

1. Hardware / Software Co- Design Principles and Practice – Jorgen Staunstrup, Wayne Wolf –2009, Springer.
2. Hardware / Software Co- Design - Giovanni De Micheli, Mariagiovanna Sami, 2002, Kluwer Academic Publishers

Reference Books

1. A Practical Introduction to Hardware/Software Co-design -Patrick R. Schaumont - springer

GOKARAJU RANGARAJU INSTITUTE OF ENGINEERING AND TECHNOLOGY

ANALOG CMOS IC DESIGN LAB

Course Code: GR18D5094 **L/T/P/C: 0/0/4/2**

Course objectives

- To describe over view about evolution of CMOS integrated circuits.
- To provide knowledge about fabrication process and technology
- To introduce and familiarize with the various Amplifiers &OP-amps
- To prepare them to face the challenges in CMOS technology

Course outcomes

- Able to develop an in-depth understanding of the design principles and applications of CMOS analog IC design.
- An ability to know the fabrication steps involved in CMOS technology.
- Familiar with the small signal and large signal models of CMOS transistors.
- An in-depth knowledge of applying the concepts on real time applications.
- Analyze and design of CMOS op Amps and compensation techniques.

Task1
Analyze the NMOS and PMOS Operating point Characteristics.
Task2
Design a CMOS Current Mirror and find out the AC, DC, OP analysis.
Task3
Design a NMOS Differential Amplifier and find out the AC, DC, OP analysis.
Task4
Design a PMOS Differential Amplifier and find out the AC, DC, OP analysis.
Task5
Design a CMOS Operational Amplifier and find out the AC analysis and noise margin analysis.
Task6
Design a comparator using Operational Amplifier and find out the AC analysis.
Task7
Draw the Analog Layout for CMOS current Mirror and perform DRC, LVS, RC Extraction.

Note: All the following digital circuits are to be designed and implemented using Cadence/ Mentor Graphics/ Synopsys/ equivalent CAD Tools.

GOKARAJU RANGARAJU INSTITUTE OF ENGINEERING AND TECHNOLOGY

ASIC DESIGN LAB

Course Code: GR18D5095 **L/T/P/C: 0/0/4/2**

Task1

Develop Verification environment using system Verilog for any one digital system.

Task2

Design and analyze the performance with respect to area, power and speed for different Adders using ASIC Logic Design Tools.

Task3

Design and analyze the performance with respect to area, power and speed for different Multipliers using ASIC Logic Design Tools.

Task4

Perform Synthesis for any digital system to meet the given specifications.

Task5

Perform Static Timing Analysis for any digital system to meet the given specifications.

Task6

Perform Floor planning, , clock tree synthesis, Placement and Routing, RC extraction for given netlist to meet the specifications.

Note: All the following digital circuits are to be designed and implemented using Cadence/ Mentor Graphics/ Synopsys/ equivalent CAD Tools.

GOKARAJU RANGARAJU INSTITUTE OF ENGINEERING AND TECHNOLOGY
ADVANCED COMPUTER ARCHITECTURE

Course Code: GR18D5096 **L/T/P/C: 3/0/0/3**

Course objectives

- To learn how to build the best processor/computing system understanding the underlying tradeoffs and ramifications.
- To identify and analyze the attributes of computer architecture design with recent trend technology.
- To identify the techniques to improve the speed and performance of computers – Parallelism in Instruction level – Hardware approaches – pipelining, dynamic scheduling, superscalar processors, and multiple issue of instructions.
- To implement the design aspects and categorize various issues, causes and hazards due to parallelisms.
- To examine and compare the performance with benchmark standards.

Course outcomes

- An ability to discuss the organization of computer-based systems and how a range of design choices are influenced by applications.
- An ability to understand the components and operation of a memory hierarchy and the range of performance issues influencing its design.
- An ability to interpret the organization and operation of current generation parallel computer systems, including multiprocessor and multicore systems.
- An ability to understand the various techniques to enhance a processors ability to exploit instruction-level parallelism (ILP), and its challenges.
- An ability to undertake performance comparisons of modern and high performance computers.

Unit I: FUNDAMENTALS OF COMPUTER DESIGN

Fundamentals of Computer design, Changing faces of computing and task of computer designer, Technology trends, Cost price and their trends, measuring and reporting performance, Quantitative principles of computer design, Amdahl's law. Instruction set principles and examples- Introduction, classifying instruction set- memory addressing type and size of operands, Operations in the instruction set.

Unit II: PIPELINES

Introduction, basic RISC instruction set, Simple implementation of RISC instruction set, Classic five stage pipe lined RISC processor, Basic performance issues in pipelining, Pipeline hazards, Reducing pipeline branch penalties. Memory Hierarchy Design: Introduction, review of ABC of cache, Cache performance, Reducing cache miss penalty, Virtual memory.

Unit III: INSTRUCTION LEVEL PARALLELISM (ILP) - THE HARDWARE APPROACH

Instruction-Level parallelism, Dynamic scheduling, Dynamic scheduling using Tomasulo's approach, Branch prediction, High performance instruction delivery- Hardware based speculation.

ILP Software Approach:

Basic compiler level techniques, Static branch prediction, VLIW approach, Exploiting ILP, Parallelism at compile time, Cross cutting issues - Hardware verses Software.

Unit IV: MULTI PROCESSORS AND THREAD LEVEL PARALLELISM

Multi Processors and Thread level Parallelism- Introduction, Characteristics of application domain, Systematic shared memory architecture, Distributed shared – Memory architecture, Synchronization.

Unit V: INTER CONNECTION AND NETWORKS

Introduction, Interconnection network media, Practical issues in interconnecting networks, Examples of inter connection, Cluster, Designing of clusters.

Intel Architecture: Intel IA-64 ILP in embedded and mobile markets Fallacies and pit falls.

Text Books

1. John L. Hennessy, David A. Patterson - Computer Architecture: A Quantitative Approach, 3rd Edition, an Imprint of Elsevier.

Reference Books

1. John P. Shen and Miikko H. Lipasti -, Modern Processor Design : Fundamentals of Super Scalar Processors
2. Computer Architecture and Parallel Processing - Kai Hwang, Faye A.Brigs., MC Graw Hill.

GOKARAJU RANGARAJU INSTITUTE OF ENGINEERING AND TECHNOLOGY

CAD FOR VLSI

Course Code: GR18D5097 **L/T/P/C: 3/0/0/3**

Course objectives

- To provide an introduction to the fundamentals of Computer-Aided Design tools for the modeling, design, analysis, test, and verification of digital Very Large Scale Integration (VLSI) systems.
- To study various physical design methods in VLSI.
- To understand the concepts behind the VLSI design rules and routing techniques.
- To use the simulation techniques at various levels in VLSI design flow.
- To understand the concepts of various algorithms used for floor planning and routing techniques.

Course outcome

- Establish comprehensive understanding of the various phases of CAD for digital electronic systems, from digital logic simulation to physical design, including test and verification.
- Demonstrate knowledge and understanding of fundamental concepts in CAD and to establish capability for CAD tool development and enhancement.
- To practice the application of fundamentals of VLSI technologies
- Optimize the implemented design for area, timing and power by applying suitable constraints.
- To gain knowledge on the methodologies involved in design, verification and implementation of digital designs on reconfigurable hardware platform(FPGA)

Unit I: VLSI PHYSICAL DESIGN AUTOMATION

VLSI Design Cycle, New Trends in VLSI Design Cycle, Physical Design Cycle, New Trends in Physical Design Cycle, Design Styles, System Packaging Styles

Unit II: PARTITIONING, FLOOR PLANNING, PIN ASSIGNMENT AND PLACEMENT

Partitioning – Problem formulation, Classification of Partitioning algorithms, Kernighan-Lin Algorithm, Simulated Annealing, Floor Planning – Problem formulation, Classification of floor planning algorithms, constraint based floor planning, Rectangular Dualization, Pin Assignment – Problem formulation, Classification of pin assignment algorithms, General and channel Pin assignments, Placement – Problem formulation, Classification of placement algorithms, Partitioning based placement algorithms.

Unit III: GLOBAL ROUTING AND DETAILED ROUTING

Global Routing – Problem formulation, Classification of global routing algorithms, Maze routing algorithms, Detailed Routing – Problem formulation, Classification of routing algorithms, Single layer routing algorithms.

Unit IV:

Physical Design Automation of FPGAs
FPGA Technologies, Physical Design cycle for FPGAs, Partitioning, Routing – Routing Algorithm for the Non-Segmented model, Routing Algorithms for the Segmented Model.
Physical Design Automation of MCMs
Introduction to MCM Technologies, MCM Physical Design Cycle.

Unit V: CHIP INPUT AND OUTPUT CIRCUITS

ESD Protection, Input Circuits, Output Circuits and noise, On-chip clock Generation and Distribution, Latch-up and its prevention.

Text Books

1. Algorithms for VLSI Physical Design Automation by Naveed Shervani, 3rd Edition, 2005, Springer International Edition.
2. CMOS Digital Integrated Circuits Analysis and Design – Sung-Mo Kang, Yusuf Leblebici, TMH, 3rd Ed., 2011.

Reference Books

1. VLSI Physical Design Automation-Theory and Practice by Sadiq M Sait, Habib Youssef, World Scientific.
2. Algorithms for VLSI Design Automation, S. H. Gerez, 1999, Wiley student Edition, John Wiley and Sons (Asia) Pvt. Ltd.
3. VLSI Physical Design Automation by Sung Kyu Lim, Springer International Edition.

GOKARAJU RANGARAJU INSTITUTE OF ENGINEERING AND TECHNOLOGY

CMOS MIXED SIGNAL CIRCUIT DESIGN

Course Code: GR18D5098 **L/T/P/C: 3/0/0/3**

Course objectives

- This course provides the concepts of switched capacitor circuits used in mixed signal circuit design.
- To know mixed signal circuits like DAC,ADC,PLL etc.,
- To acquire knowledge on design different architectures in mixed signal mode.
- To gain knowledge on noise shaping modulators and higher order modulators.
- It deals with the design and analysis of Biquad Filters.

Course outcomes

- Analyze and design of switched capacitor circuits used in mixed signal circuit design
- Design noise shaping converters given a set of requirements such as bandwidth, clock speed and signal-to-noiseratio
- Design an integrated mixed signal circuit in CMOS using modern design tools
- Demonstrate in-depth knowledge in PLL and Data Converters (DAC and ADC)
- Analyze complex engineering problems critically for conducting research in data converters

Unit I: SWITCHED CAPACITOR CIRCUITS

Introduction to Switched Capacitor circuits- basic building blocks, Operation and Analysis, Non-ideal effects in switched capacitor circuits, Switched capacitor integrators first order filters, Switch sharing, biquad filters.

Unit II: PHASED LOCK LOOP (PLL)

Basic PLL topology, Dynamics of simple PLL, Charge pump PLLs-Lock acquisition, Phase/Frequency detector and charge pump, Basic charge pump PLL, Non-ideal effects in PLLs-PFD/CP non-idealities, Jitter in PLLs, Delay locked loops, applications

Unit III: DATA CONVERTER FUNDAMENTALS

DC and dynamic specifications, Quantization noise, Nyquist rate D/A converters- Decoder based converters, Binary-Scaled converters, Thermometer-code converters, Hybrid converters.

Unit IV: NYQUIST RATE A/D CONVERTERS

Successive approximation converters, Flash converter, Two-step A/D converters, Interpolating A/D converters, Folding A/D converters, Pipelined A/D converters, Time-interleaved converters.

Unit V: OVERSAMPLING CONVERTERS

Noise shaping modulators, Decimating filters and interpolating filters, Higher order modulators, Delta sigma modulators with multibit quantizes, Delta sigma D/A

Text Books

1. Design of Analog CMOS Integrated Circuits- Behzad Razavi, TMH Edition, 2002
2. CMOS Analog Circuit Design - Philip E. Allen and Douglas R. Holberg, Oxford University Press, International Second Edition/Indian Edition, 2010.
3. Analog Integrated Circuit Design- David A. Johns,Ken Martin, Wiley Student Edition, 2013

Reference Books

1. CMOS Integrated Analog-to- Digital and Digital-to-Analog converters-Rudy Van De Plassche, Kluwer Academic Publishers, 2003
2. Understanding Delta-Sigma Data converters-Richard Schreier, Wiley Inderscience, 2005.
3. CMOS Mixed-Signal Circuit Design - R. Jacob Baker, Wiley Inderscience, 2009.

GOKARAJU RANGARAJU INSTITUTE OF ENGINEERING AND TECHNOLOGY

BUSINESS ANALYTICS

Course Code: GR18D5201 **L/T/P/C: 3/0/0/3**

Course objectives

- Understand the role of business analytics and statistical tools used within an organization.
- Discuss Trendiness and Regression Analysis and different visualization techniques to explore data.
- Describe the organization structure and different type of business analytics.
- Know Forecasting Techniques, Monte Carlo Simulation and Risk Analysis.
- Understanding decision analysis and recent trends in business intelligence.

Course Outcomes

- Demonstrate business analytics process and use statistical tools for implementation of business process.
- Design relationships and trends to explore and visualize the data.
- Examine the organization structure of business analytics and categorize types of analytics.
- Apply forecasting techniques, monte carlo simulation and risk analysis.
- Formulate decision analysis and summarize recent trends in business intelligence.

Unit I

Optimization Techniques, Model Formulation, models, General L.R Formulation, Simplex

Techniques, Sensitivity Analysis, Inventory Control Models.

Unit II

Formulation of a LPP - Graphical solution revised simplex method - duality theory - dual simplex method - sensitivity analysis - parametric programming.

Unit III

Nonlinear programming problem - Kuhn-Tucker conditions min cost flow problem - max flow problem - CPM/PERT

Unit IV

Scheduling and sequencing - single server and multiple server models - deterministic inventory models - Probabilistic inventory control models - Geometric Programming.

Unit V

Competitive Models, Single and Multi-channel Problems, Sequencing Models, Dynamic Programming, Flow in Networks, Elementary Graph Theory, Game Theory Simulation.

Reference Books

1. H.A. Taha, Operations Research, An Introduction, PHI,2008
2. Wagner, Principles of Operations Research, PHI, Delhi,1982.
3. J.C. Pant, Introduction to Optimization: Operations Research, Jain Brothers, Delhi,2008
4. Hitler Libermann Operations Research: McGraw Hill Pub.2009
5. Pannerselvam, Operations Research: Prentice Hall of India2010
6. Harvey M Wagner, Principles of Operations Research: Prentice Hall of India2010

GOKARAJU RANGARAJU INSTITUTE OF ENGINEERING AND TECHNOLOGY

INDUSTRIAL SAFETY

Course Code: GR18D5202 **L/T/P/C: 3/0/0/3**

Course Objectives

- To understand the importance of maintaining a safe workplace.
- To maintain safety standards in compliance with regulatory requirements and within engineering limits understand personal safety and industrial safety.
- To create a job safety analysis (JSA) for a given work project.
- To follow safety recordkeeping and management, and the role of the safety manager.
- To utilize personal proactive equipment.

Course outcomes: After successful completion of the course the student will be able to

- Understanding of safety principles.
- Analyze different types of exposure and biological effects, exposure guidelines and basic workplace monitoring ability to do hazard analysis.
- Demonstrate an understanding of workplace injury prevention, risk management, and incident investigations.
- Understand the acute and chronic health effects of exposure to chemical, physical and biological agents in the workplace.
- Demonstrate knowledge of the types of hazards, planning, organization and training needed to work safely with hazardous materials.

Unit I: INDUSTRIAL SAFETY

Accident, causes, types, results and control, mechanical and electrical hazards, types, causes and preventive steps/procedure, describe salient points of factories act 1948 for health and safety, wash rooms, drinking water layouts, light, cleanliness, fire, guarding, pressure vessels, etc, Safety color codes. Fire prevention and firefighting, equipment and methods.

Unit II: FUNDAMENTALS OF MAINTENANCE ENGINEERING

Definition and aim of maintenance engineering, Primary and secondary functions and responsibility of maintenance department, Types of maintenance, Types and applications of tools used for maintenance, Maintenance cost & its relation with replacement economy, Service life of equipment.

Unit III: WEAR AND CORROSION AND THEIR PREVENTION

Wear- types, causes, effects, wear reduction methods, lubricants-types and applications, Lubrication methods, general sketch, working and applications, i. Screw down grease cup, ii. Pressure grease gun, iii. Splash lubrication, iv. Gravity lubrication, v. Wick feed lubrication vi. Side feed lubrication, vii. Ring lubrication, Definition, principle and factors affecting the corrosion. Types of corrosion, corrosion prevention methods.

Unit IV: FAULT TRACING

Fault tracing-concept and importance, decision tree concept, need and applications, sequence of fault finding activities, show as decision tree, draw decision tree for problems in machine tools, hydraulic, pneumatic ,automotive, thermal and electrical equipment's like, I. Any one Machine tool, ii. Pump iii. Air compressor, iv. Internal combustion engine, v. Boiler, vi. Electrical motors, Types of faults in machine tools and their general causes.

Unit V: PERIODIC AND PREVENTIVE MAINTENANCE

Periodic inspection-concept and need, degreasing, cleaning and repairing schemes, overhauling of mechanical components, overhauling of electrical motor, common troubles and remedies of electric motor, repair complexities and its use, definition, need, steps and advantages of preventive maintenance. Steps/procedure for periodic and preventive maintenance of: I. Machine tools, ii. Pumps, iii. Air compressors, iv. Diesel generating (DG) sets, Program and schedule of preventive maintenance of mechanical and electrical equipment, advantages of preventive maintenance. Repair cycle concept and importance

Reference Books

1. Maintenance Engineering Handbook, Higgins & Morrow, Da Information Services.
2. Maintenance Engineering, H. P. Garg, S. Chand and Company.
3. Pump-hydraulic Compressors, Audels, Mcgrew Hill Publication.
4. Foundation Engineering Handbook, Winterkorn, Hans, Chapman & Hall London.

GOKARAJU RANGARAJU INSTITUTE OF ENGINEERING AND TECHNOLOGY

OPERATIONS RESEARCH

Course Code: GR18D5203 **L/T/P/C: 3/0/0/3**

Course objectives

- To define and formulate linear and non-linear programming problems and appreciate their limitations arising from a wide range of applications.
- To perform sensitivity analysis to determine the direction and magnitude of change of a model s optimal solution as the data change.
- To distinguish various inventory models and develop proper inventory policies.
- To solve the scheduling and sequencing models.
- To understand how to model and solve problems using dynamic programming, game theory.

Course Outcomes

- The student will formulate and solve problems as networks and graphs for optimal allocation of limited resources such as machine, material and money.
- The student will able to carry out sensitivity analysis.
- The student will solve network models like the shortest path, minimum spanning tree, And maximum flow problems.
- The student will able to distinguish various inventory models and develop proper inventory policies.
- The student will also propose the best strategy using decision making methods under uncertainty and game theory.

Unit I

Optimization Techniques, Model Formulation, models, General L.R Formulation, Simplex Techniques, Sensitivity Analysis, Inventory Control Models.

Unit II

Formulation of a LPP - Graphical solution revised simplex method - duality theory - dual simplex method - sensitivity analysis - parametric programming.

Unit III

Nonlinear programming problem - Kuhn-Tucker conditions min cost flow problem - max flow problem - CPM/PERT

Unit IV

Scheduling and sequencing - single server and multiple server models - deterministic inventory models - Probabilistic inventory control models - Geometric Programming.

Unit V

Competitive Models, Single and Multi-channel Problems, Sequencing Models, Dynamic

Programming, Flow in Networks, Elementary Graph Theory, Game Theory Simulation.

Reference Books

1. H.A. Taha, Operations Research, An Introduction, PHI,2008
2. Wagner, Principles of Operations Research, PHI, Delhi,1982.
3. J.C. Pant, Introduction to Optimization: Operations Research, Jain Brothers, Delhi,2008
4. Hitler Libermann Operations Research: McGraw Hill Pub.2009
5. Pannerselvam, Operations Research: Prentice Hall of India2010
6. Harvey M Wagner, Principles of Operations Research: Prentice Hall of India2010

GOKARAJU RANGARAJU INSTITUTE OF ENGINEERING AND TECHNOLOGY

COST MANAGEMENT OF ENGINEERING PROJECTS

Course Code: GR18D5204 **L/T/P/C: 3/0/0/3**

Course Objectives

a. To provide the student with a clear understanding of strategic cost management process.
b. To describe the various stages of project execution.
c. To prepare the project schedule by bar charts and network diagram.
d. To conduct breakeven and cost-volume-profit analysis.
e. To make students various budgets and quantitative techniques used for cost management.

Course outcomes

- The student will be able to explain the various cost concepts used in decision making.
- To be able to identify and demonstrate various stages of project execution.
- The students will be able to prepare the project schedule by bar charts and network diagrams.
- The student will be to differentiate absorption costing and marginal costing, also conduct breakeven and cost-volume-profit analysis.
- The student will be able to prepare various budgets and quantitative techniques used for cost management.

Unit I

Introduction and Overview of the Strategic Cost Management Process, Cost concepts in decision-making; relevant cost, Differential cost, Incremental cost and Opportunity cost. Objectives of a Costing System; Inventory valuation; Creation of a Database for operational control; Provision of data for Decision-Making.

Unit II

Project: meaning, Different types, why to manage, cost overruns centers, various stages of project execution: conception to commissioning. Project execution as conglomeration of technical and non- technical activities. Detailed Engineering activities. Pre project execution main clearances and documents Project team: Role of each member. Importance Project site: Data required with significance. Project contracts. Types and contents. Project execution Project cost control. Bar charts and Network diagram. Project commissioning: mechanical and process

Unit III

Cost Behavior and Profit Planning Marginal Costing; Distinction between Marginal Costing and Absorption Costing; Break-even Analysis, Cost-Volume-Profit Analysis. Various decision-making problems. Standard Costing and Variance Analysis. Pricing strategies: Pareto Analysis. Target costing, Life Cycle Costing. Costing of service sector. Just-in-time approach, Material Requirement Planning, Enterprise Resource Planning, Total Quality Management and Theory of constraints. Activity-Based Cost Management, Bench Marking; Balanced Score Card and Value-Chain Analysis.

Unit IV

Budgetary Control; Flexible Budgets; Performance budgets; Zero-based budgets. Measurement of Divisional profitability pricing decisions including transfer pricing.

Unit V

Quantitative techniques for cost management, Linear Programming, PERT/CPM, Transportation problems, Assignment problems, Simulation, Learning Curve Theory.

Reference Books

1. Cost Accounting A Managerial Emphasis, Prentice Hall of India, New Delhi.
2. Charles T. Horngren and George Foster, Advanced Management Accounting.
3. Robert S Kaplan Anthony A. Alkinson, Management & Cost Accounting.
4. Ashish K. Bhattacharya, Principles & Practices of Cost Accounting A. H. Wheeler publisher.
5. N.D. Vohra, Quantitative Techniques in Management, Tata McGraw Hill Book Co.Ltd.

GOKARAJU RANGARAJU INSTITUTE OF ENGINEERING AND TECHNOLOGY

COMPOSITE MATERIALS

Course Code: GR18D5205 **L/T/P/C: 3/0/0/3**

Course objectives: The objectives of this course is to provide the students,

- To understand the concepts of fundamental science and engineering principles relevant to materials engineering.
- To expose the various methods to test mechanical properties on materials.
- To categorize the various equilibrium diagrams and describe the changes which occurs on metals.
- To explain the concepts on various heat treatment operations.
- To explain the various ferrous and non-ferrous metals with their properties and applications.

Course outcomes: At the end of the course, students will be able to

- Relate crystal structures and identify the relation between different materials.
- Test the various mechanical properties of metal by suitable method.
- Relate the equilibrium transformation diagram for various ferrous and non-ferrous metals.
- Utilize appropriate techniques in treating with proper heat treatment operation.
- Evaluate the behavior of material when it subjected to heat treatment process.

Unit I: INTRODUCTION

Definition – Classification and characteristics of Composite materials. Advantages and application of composites. Functional requirements of reinforcement and matrix. Effect of reinforcement (size, shape, distribution, volume fraction) on overall composite performance.

Unit II: REINFORCEMENTS

Preparation-layup, curing, properties and applications of glass fibers, carbon fibers, Kevlar fibers and Boron fibers. Properties and applications of whiskers, particle reinforcements. Mechanical Behavior of composites: Rule of mixtures, Inverse rule of mixtures. Isostrain and Isostress conditions.

Unit III: MANUFACTURING OF METAL MATRIX COMPOSITES

Casting – Solid State diffusion technique, Cladding – Hot isostatic pressing. Properties and applications. Manufacturing of Ceramic Matrix Composites: Liquid Metal Infiltration – Liquid phase sintering. Manufacturing of Carbon – Carbon composites: Knitting, Braiding, Weaving. Properties and applications.

Unit IV: MANUFACTURING OF POLYMER MATRIX COMPOSITES

Preparation of Moulding compounds and prepregs – hand layup method – Autoclave method – Filament winding method – Compression moulding – Reaction injection moulding. Properties and applications.

Unit V: STRENGTH

Laminar Failure Criteria-strength ratio, maximum stress criteria, maximum strain criteria, interacting failure criteria, hygrothermal failure. Laminate first play failure-insight strength; Laminate strength-ply discount truncated maximum strain criterion; strength design using caplet plots; stress concentrations.

Text Books

1. Material Science and Technology – Vol 13 – Composites by R.W.Cahn – VCH, West Germany.
2. Materials Science and Engineering, An introduction. WD Callister, Jr., Adapted by R. Balasubramaniam, John Wiley & Sons, NY, Indian edition,2007.

Reference Books

1. Hand Book of CompositeMaterials-ed-Lubin.
2. Composite Materials –K.K.Chawla.
3. Composite Materials Science and Applications – Deborah D.L.Chung.
4. Composite Materials Design and Applications – Danial Gay, Suong V. Hoa, and Stephen W.Tasi.

GOKARAJU RANGARAJU INSTITUTE OF ENGINEERING AND TECHNOLOGY

WASTE TO ENERGY

Course Code: GR18D5206 **L/T/P/C: 3/0/0/3**

Course Objectives

- To find or recall the non-hazardous secondary materials from waste.
- To compare precisely to overcome the cost and most economically attractive course of action for CH4 emission.
- To demonstrate the techno-economic feasibility of replacing.
- To extend the students for possible future activity in a biomass plant.
- To utilization in spark-ignited internal combustion engine.

Course outcomes

- Students are able to make use of energy installation and the small of household bio-waste incineration.
- To develop actual dimension must of course, fit requirement of the masonry block.
- To become capable of analyze and design of energy conversion system.
- Students are to estimate the possibility of invest in biomass generation.
- Students will be able to explain the biogas its uses and benefits.

Unit I: INTRODUCTION TO ENERGY FROM WASTE

Classification of waste as fuel – Agro based, Forest residue, Industrial waste - MSW – Conversion devices – Incinerators, gasifiers, digestors

Unit II : BIOMASS PYROLYSIS

Pyrolysis – Types, slow fast – Manufacture of charcoal – Methods - Yields and application – Manufacture of pyrolytic oils and gases, yields and applications.

Unit III : BIOMASS GASIFICATION

Gasifiers – Fixed bed system – Downdraft and updraft gasifiers – Fluidized bed gasifiers – Design, construction and operation – Gasifier burner arrangement for thermal heating – Gasifier engine arrangement and electrical power – Equilibrium and kinetic consideration in gasifier operation.

Unit IV : BIOMASS COMBUSTION

Biomass stoves – Improved chullahs, types, some exotic designs, Fixed bed combustors,

Types, inclined grate combustors, Fluidized bed combustors, Design, construction and operation - Operation of all the above biomass combustors.

Unit V: BIOGAS

Properties of biogas (Calorific value and composition) - Biogas plant technology and status - Bio energy system - Design and constructional features - Biomass resources and their classification - Biomass conversion processes - Thermo chemical conversion - Direct combustion - biomass gasification - pyrolysis and liquefaction - biochemical conversion - anaerobic digestion - Types of biogas Plants – Applications - Alcohol production from biomass - Bio diesel production - Urban waste to energy conversion - Biomass energy programme in India.

Reference Books

1. Non-Conventional Energy, Desai, Ashok V., Wiley Eastern Ltd.,1990.
2. Biogas Technology - A Practical Hand Book - Khandelwal, K. C. and Mahdi, S. S., Vol. I & II, Tata McGraw Hill Publishing Co. Ltd.,1983.
3. Food, Feed and Fuel from Biomass, Challal, D. S., IBH Publishing Co. Pvt. Ltd.,1991.
4. Biomass Conversion and Technology, C. Y. WereKo-Brobby and E. B. Hagan, John Wiley & Sons, 1996.

GOKARAJU RANGARAJU INSTITUTE OF ENGINEERING AND TECHNOLOGY

ENGLISH FOR RESEARCH PAPER WRITING

Course Code: GR18D5207 **L/T/P/C: 2/0/0/2**

Course objectives

- To state how to put research on paper
- To demonstrate how to write an abstract
- To apply the process of research
- To appraise the key skills involved in writing the title, abstract, introduction and review of literature
- To compose a paper which is good and has the qualities of acceptance and publication

Course Outcomes

- Will be able to understand how to write a research paper
- Will outline the drafting of an abstract
- Will acquire the skills of various elements of research
- Will be in a position to write a good paper
- Will result in increasing the chance of publication

Unit I

Planning and Preparation, Word Order, Breaking up long sentences, Structuring Paragraphs and Sentences, Being Concise and Removing Redundancy, Avoiding Ambiguity and Vagueness.

Unit II

Clarifying Who DidWhat, Highlighting Your Findings, Hedging and Criticising, Paraphrasing and Plagiarism, Sections of a Paper, Abstracts, Introduction.

Unit III

Review of the Literature, Methods, Results, Discussion, Conclusions, TheFinal Check.

Unit IV

Key skills are needed when writing a Title, key skills are needed whenwriting an Abstract,

key skills are needed when writing an Introduction, skills needed when writing a Review of the Literature.

Unit V

Skills are needed when writing the Methods, skills needed when writing the Results, skills are needed when writing the Discussion, skills are needed when writing the Conclusion.

Reference Books

1. Goldbort R (2006) Writing for Science, Yale University Press (available on GoogleBooks)
2. Day R (2006) How to Write and Publish a Scientific Paper, Cambridge UniversityPress
3. Highman N (1998), Handbook of Writing for the Mathematical Sciences, SIAM. Highman's book.
4. Ian Wallwork , English for Writing Research Papers, Springer New York Dordrecht Heidelberg London, 2011.

GOKARAJU RANGARAJU INSTITUTE OF ENGINEERING AND TECHNOLOGY

DISASTER MANAGEMENT

Course Code: GR18D5208 **L/T/P/C: 2/0/0/2**

Course objectives

- Learn to demonstrate a critical understanding of key concepts in disaster risk reduction and humanitarian response.
- Critically evaluate disaster risk reduction and humanitarian response policy and practice from multiple perspectives.
- Develop an understanding of standards of humanitarian response and practical relevance in specific types of disasters and conflict situations.
- Critically understand the strengths and weaknesses of disaster management approaches,
- Planning and programming in different countries, particularly their home country or the countries they work in.

Course Outcomes

- Capacity to integrate knowledge and to analyze, evaluate and manage the different public health aspects of disaster events at a local and global levels, even when limited information is available.
- Capacity to describe, analyze and evaluate the environmental, social, cultural, economic, legal and organizational aspects influencing vulnerabilities and capacities to face disasters.
- Capacity to work theoretically and practically in the processes of disaster management (disaster risk reduction, response, and recovery) and relate their interconnections, particularly in the field of the Public Health aspects of the disasters.
- Capacity to manage the Public Health aspects of the disasters.
- Capacity to obtain, analyze, and communicate information on risks, relief needs and lessons learned from earlier disasters in order to formulate strategies for mitigation in future scenarios with the ability to clearly present and discuss their conclusions and the knowledge and arguments behind them.

Unit I: INTRODUCTION

Disaster: Definition, Factors and Significance; Difference between Hazard and Disaster; Natural and Manmade Disasters: Difference, Nature, Typesand Magnitude.

Unit II: REPERCUSSIONS OF DISASTERS AND HAZARDS

Economic Damage, Loss of Human and Animal Life, Destruction of Ecosystem. **Natural Disasters**: Earthquakes, Volcanisms, Cyclones, Tsunamis, Floods, Droughts andFamines, Landslides and Avalanches, Man-made disaster: Nuclear Reactor Meltdown, Industrial Accidents, Oil Slicks and Spills, Outbreaks of Disease and Epidemics, War and Conflicts.

Unit III: DISASTER PRONE AREAS IN INDIA

Study of Seismic Zones; Areas Prone To Floods and Droughts, Landslides and Avalanches; Areas Prone To Cyclonic and Coastal Hazards with Special Reference to Tsunami; Post-Disaster Diseases and Epidemics

Unit IV: DISASTER PREPAREDNESS AND MANAGEMENT

Preparedness: Monitoring Of Phenomena Triggering A Disaster Or Hazard; Evaluation Of Risk: Application Of Remote Sensing, Data From Meteorological And Other Agencies, Media Reports: Governmental And Community Preparedness.

Unit V: RISK ASSESSMENT

Disaster Risk: Concept and Elements, Disaster Risk Reduction, Global and National Disaster Risk Situation. Techniques of Risk Assessment, Global Co- Operation in Risk Assessment and Warning, People's Participation in Risk Assessment. Strategies for Survival.

Reference Books

1. R. Nishith, Singh AK, "Disaster Management in India: Perspectives, issues and strategies "'New Royal bookCompany
2. Sahni, Pardeep Et.Al. (Eds.)," Disaster Mitigation Experiences and Reflections", Prentice Hall Of India, NewDelhi.
3. Goel S. L., Disaster Administration And Management Text And Case Studies" ,Deep &Deep Publication Pvt. Ltd., NewDelhi.

GOKARAJU RANGARAJU INSTITUTE OF ENGINEERING AND TECHNOLOGY

SANSKRIT FOR TECHNICAL KNOWLEDGE

Course Code: GR18D5209 **L/T/P/C: 2/0/0/2**

Course objectives

- To get a working knowledge in illustrious Sanskrit, the scientific language in the world.
- Learning of Sanskrit to improve brain functioning.
- Learning of Sanskrit to develop the logic in mathematics, science & other subjects.
- Enhancing the memory power.
- The engineering scholars equipped with Sanskrit will be able to explore the huge knowledge from ancient literature.

Course Outcomes

- Understanding basic Sanskrit alphabets and Understand tenses in Sanskrit Language.
- Enable students to understand roots of Sanskrit language.
- Students learn engineering fundamentals in Sanskrit.
- Students can attempt writing sentences in Sanskrit.
- Ancient Sanskrit literature about science & technology can be under stood

Unit I

Alphabets in Sanskrit, Past/Present/Future Tense, Simple Sentences

Unit II

Order, Introduction of roots, Technical information about Sanskrit Literature

Unit III

Technical concepts of Engineering-Electrical, Mechanical, Architecture, Mathematics

Reference Books

1. "Abhyaspustakam" – Dr.Vishwas, Samskrita-Bharti Publication, NewDelhi
2. "Teach Yourself Sanskrit" Prathama Deeksha-Vempati Kutumbshastri, Rashtriya Sanskrit Sansthanam, New DelhiPublication
3. "India's Glorious Scientific Tradition" Suresh Soni, Ocean books (P) Ltd., NewDelhi.

GOKARAJU RANGARAJU INSTITUTE OF ENGINEERING AND TECHNOLOGY

VALUE EDUCATION

Course Code: GR18D5210 **L/T/P/C: 2/0/0/2**

Course objectives

- Understand value of education and self-development.
- Imbibe good values in students.
- Let the should know about the importance of character.
- To understand the significance of human conduct and self-development.
- To enable students to imbibe and internalize the value and Ethical behaviour in personal and professional lives.

Course outcomes

- Knowledge of self-development.
- Learn the importance of Human values.
- Developing the overall personality.
- Student will be able to realize the significance of ethical human conduct and self-development.
- Students will be able to inculcate positive thinking, dignity of labour and religiou tolerance.

Unit I

Values and self-development –Social values and individual attitudes, Work ethics, Indian vision of humanism, Moral and non- moral valuation, Standards andprinciples, Value judgement.

Unit II

Importance of cultivation of values, Sense ofduty. Devotion, Self-reliance. Confidence, Concentration. Truthfulness, Cleanliness. Honesty, Humanity. Power of faith, NationalUnity. Patriotism. Love for nature, Discipline

Unit III

Personality and Behavior Development - Soul and Scientific attitude, Positive Thinking, Integrity and discipline, Punctuality, Love and Kindness, Avoid fault Thinking, Free from anger, Dignity of labour, Universal brotherhood and religious tolerance, True friendship, Happiness vs suffering, love for truth, Aware of self-destructive habits, Association and Cooperation, Doing best for saving nature.

Unit IV

Character and Competence –Holy books vs Blindfaith. Self-management and Goodhealth.

Science of reincarnation. Equality, Nonviolence, Humility, Role ofWomen. All religions and same message. Mind your Mind,Self-control. Honesty, Studyingeffectively

Reference Books

1. Chakroborty, S.K. “Values and Ethics for organizations Theory and practice”, Oxford University Press, New Delhi.

GOKARAJU RANGARAJU INSTITUTE OF ENGINEERING AND TECHNOLOGY
INDIAN CONSTITUTION

Course Code: GR18D5211 **L/T/P/C: 2/0/0/2**

Course objectives

- Understand the premises informing the twin themes of liberty and freedom from a civil rights perspective.
- To address the growth of Indian opinion regarding modern Indian intellectuals' constitutional
- Role and entitlement to civil and economic rights as well as the emergence of nationhood in the early years of Indian nationalism.
- To address the role of socialism in India after the commencement of the Bolshevik Revolution in 1917 and its impact on the initial drafting of the Indian Constitution.
- To understand the role and functioning of Election Commission of India.

Course outcomes

- Discuss the growth of the demand for civil rights in India for the bulk of Indians before the arrival of Gandhi in Indian politics.
- Discuss the intellectual origins of the framework of argument that informed the conceptualization of social reforms leading to revolution in India.
- Discuss the circumstances surrounding the foundation of the Congress Socialist Party [CSP] under the leadership of Jawaharlal Nehru and the eventual failure of the proposal of direct elections through adult suffrage in the Indian Constitution.
- Discuss the passage of the Hindu Code Bill of1956.
- Discuss the significance of Election Commission of India.

Unit I

History of Making of the Indian Constitution: History Drafting Committee, (Composition & Working).

Unit II

Philosophy of the Indian Constitution: Preamble Salient Features.

Unit III

Contours of Constitutional Rights &Duties: Fundamental Rights, Right to Equality, Right to Freedom, Right against Exploitation, Right to Freedom of Religion, Cultural and Educational Rights, Right to Constitutional Remedies, Directive Principles of State Policy, Fundamental Duties.

Unit IV

Organs of Governance: Parliament-Composition, Qualifications and Disqualifications, Powers and Functions, Executive, President, Governor, Council of Ministers, Judiciary, Appointment and Transfer of Judges, Qualifications, Powers and Functions.

Unit V

Local Administration: District's Administration head: Role and Importance, Municipalities: Introduction, Mayor and role of Elected Representative, CEO of MunicipalCorporation. Pachayati raj: Introduction, PRI: Zila Pachayat. Elected officials and their roles, CEO Zila Pachayat: Position androle. Block level: Organizational Hierarchy (Different departments), Village level: Role of Elected and Appointed officials, Importance of grass root democracy.

Unit VI

Election Commission: Election Commission: Role and Functioning, Chief Election Commissioner and Election Commissioners, State Election Commission: Role and Functioning, Institute and Bodies for the welfare of SC/ST/OBC and women.

Reference Books

1. The Constitution of India, 1950 (Bare Act), Government Publication.
2. Dr. S. N. Busi, Dr. B. R. Ambedkar framing of Indian Constitution, 1st Edition,2015.
3. M. P. Jain, Indian Constitution Law, 7th Edn., Lexis Nexis,2014.
4. D.D. Basu, Introduction to the Constitution of India, Lexis Nexis,2015.

GOKARAJU RANGARAJU INSTITUTE OF ENGINEERING AND TECHNOLOGY

PEDAGOGY STUDIES

Course Code: GR18D5212 **L/T/P/C: 2/0/0/2**

Course objectives

- Review existing evidence on the review topic to inform Programme design and policy making
- Undertaken by the DFID, other agencies and researchers.
- Identify critical evidence gaps to guide the development.
- Establishing coordination among people in order to execute pedagogy methods.
- To study pedagogy as a separate discipline.

Course Outcomes

- What pedagogical practices are being used by teachers in formal classrooms in developing countries?
- What pedagogical practices are being used by teachers in informal classrooms in developing countries?
- Synergy from the work force.
- What is the evidence on the effectiveness of these pedagogical practices, in what conditions, and with what population of learners?
- How can teacher education (curriculum and practicum) and the school curriculum and guidance materials best support effective pedagogy?

Unit I

Introduction and Methodology: Aims and rationale, Policy background, Conceptual framework and terminology Theories of learning, Curriculum, Teacher education. Conceptual framework, Research questions**.** Overview of methodology and Searching.

Unit II

Thematic overview: Pedagogical practices are being used by teachers in formal and informal classrooms in developing countries. Curriculum, Teacher education.

Unit III

Evidence on the effectiveness of pedagogical practices, Methodology for the in-depth stage: quality assessment of included studies. How can teacher education (curriculum and practicum) and the school curriculum and guidance materials best support effective pedagogy? Theory of change. Strength and nature of the body of evidence for effective pedagogical practices. Pedagogic theory and pedagogical approaches. Teachers' attitudes and beliefs and Pedagogic strategies.

Unit IV

Professional development: alignment with classroom practices and follow- up support, Peer support, Support from the head teacher and the community, Curriculum and assessment, Barriers to learning: limited resources and large classsizes

Unit V

Research gaps and future directions: Research design, Contexts, Pedagogy, Teacher education, Curriculum and assessment, Dissemination and research impact.

Reference Book

1. Ackers J, Hardman F (2001) Classroom interaction in Kenyan primary schools, Compare, 31 (2): 245-261.
2. Agrawal M (2004) Curricular reform in schools: The importance of evaluation, Journal of Curriculum Studies, 36 (3):361-379.
3. Akyeampong K (2003) Teacher training in Ghana - does it count? Multi-site teacher education research project (MUSTER) country report 1. London:DFID.
4. Akyeampong K, Lussier K, Pryor J, Westbrook J (2013) Improving teaching and learning of basic maths and reading in Africa: Does teacher preparation count? International Journal Educational Development, 33 (3):272–282.
5. Alexander RJ (2001) Culture and pedagogy: International comparisons in primary education. Oxford and Boston:Blackwell.
6. Chavan M (2003) Read India: A mass scale, rapid, 'learning to read'campaign.
7. www.pratham.org/images/resource%20working%20paper%202.pdf.

GOKARAJU RANGARAJU INSTITUTE OF ENGINEERING AND TECHNOLOGY

STRESS MANAGEMENT BY YOGA

Course Code: GR18D5213 **L/T/P/C: 2/0/0/2**

Course objectives

- To achieve overall Good Health of Body and Mind.
- To lower blood pressure and improve heart health.
- To become non-violent and truthfulness.
- To increase the levels of happiness.
- To eliminate all types of body pains.

Course outcomes

- Develop healthy mind in a healthy body thus improving social health also improve efficiently.
- Develop body awareness. Learn how to use their bodies in a healthy way. Perform well in sports and academics.
- Will balance, flexibility, and stamina, strengthen muscles and connective tissues enabling good posture.
- Manage stress through breathing, awareness, meditation and healthy movement.
- Build concentration, confidence and positive self-image.

Unit I

Definitions of Eight parts of yog. (Ashtanga)

Unit II

Yam and Niyam. Do`s and Don't's inlife. Ahinsa, satya, astheya, bramhacharya andaparigraha Shaucha, santosh, tapa, swadhyay,ishwarpranidhan

Unit III

Asan andPranayam, Various yog poses and their benefits for mind & body. Regulaization of breathing techniques and its effects-Types of pranayam

Reference Books

1. 'Yogic Asanas for Group Tarining-Part-I" : Janardan Swami Yogabhyasi Mandal,Nagpur
2. "Rajayoga or conquering the Internal Nature" by SwamiVivekananda, Advaita Ashrama (Publication Department),Kolkata

GOKARAJU RANGARAJU INSTITUTE OF ENGINEERING AND TECHNOLOGY

PERSONALITY DEVELOPMENT THROUGH LIFE ENLIGHTENMENT SKILLS

Course Code: GR18D5214 **L/T/P/C: 2/0/0/2**

Course objectives

- To learn to achieve the highest goal happily
- To become a person with stable mind, pleasing personality and determination
- To awaken wisdom in students
- To differentiate three types of happiness (Sukham)
- To describe the character traits of a spiritual devotee

Course outcomes

- Study of Shrimad- Bhagwad-Gita wiil help the student in developing his personality and achieve the highest goal in life
- The person who has studied Geeta will lead the nation and mankind to peace and prosperity
- To develop self-developing attitude towards work without self-aggrandizement
- To develop tranquil attitude in all favorable and unfavorable situations
- To develop high spiritual intelligence

Unit I: Neetisatakam-Holistic development of personality

- Verses- 19,20,21,22 (wisdom)
- Verses- 29,31,32 (pride &heroism)
- Verses- 26,28,63,65 (virtue)
- Verses- 52,53,59 (dont's)
- Verses- 71,73,75,78 (do's)

Unit II: Approach to day to day work andduties.

- Shrimad Bhagwad Geeta : Chapter 2-Verses 41,47,48,
- Chapter 3-Verses 13, 21, 27, 35, Chapter 6-Verses 5,13,17, 23,35,
- Chapter 18-Verses 45, 46,48.

Unit III: Statements of basicknowledge.

- Shrimad Bhagwad Geeta: Chapter2-Verses 56, 62,68
- Chapter 12 -Verses 13, 14, 15, 16,17,18
- Personality of Role model. Shrimad BhagwadGeeta: Chapter2-Verses 17, Chapter 3-Verses36,37,42,
- Chapter 4-Verses 18,38,39
- Chapter18 – Verses37,38,63

Reference Books

1. “Srimad Bhagavad Gita” by Swami Swarupananda Advaita Ashram (Publication Department),Kolkata
2. Bhartrihari’s Three Satakam (Niti-sringar-vairagya) by P.Gopinath, Rashtriya Sanskrit Sansthanam, NewDelhi.